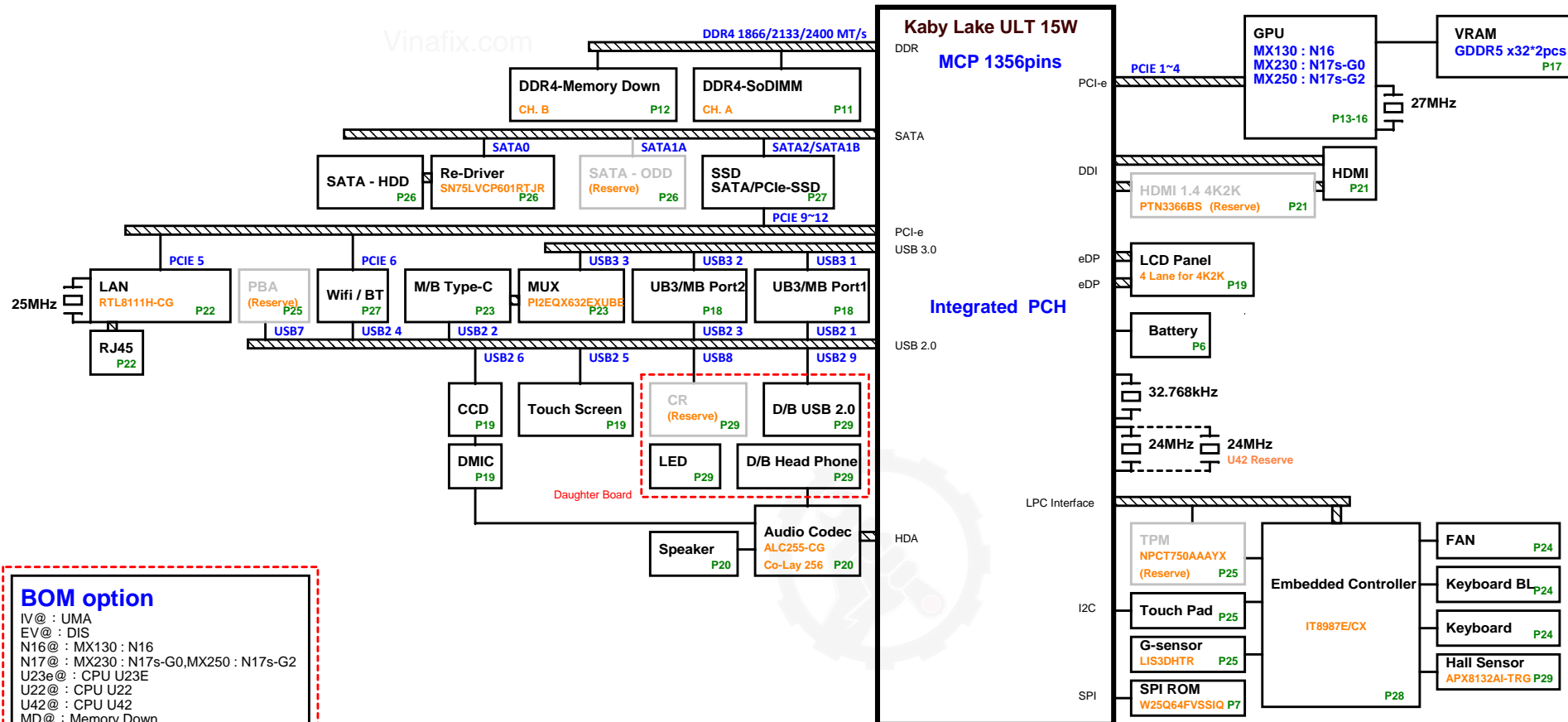


ZAUA KabyLake-U/R series Platform Block Diagram

01

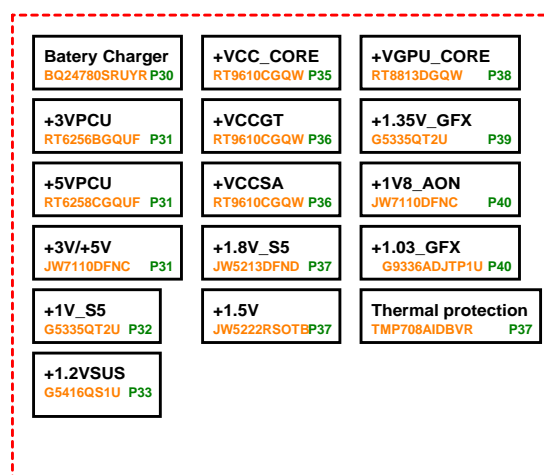
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BOM option

IV@ : UMA
 EV@ : DIS
 N16@ : MX130 : N16
 N17@ : MX230 : N17s-G0, MX250 : N17s-G2
 U23e@ : CPU U23E
 U22@ : CPU U22
 U42@ : CPU U42
 MD@ : Memory Down
 U42P@ : Power for U42
 SP@ : Power & CPU
 EV_SP@ : VGA
 SSD@ : Solid State Disk
 HDD@ : Hard Disc
 HDD_R@ : Hard Disc Redriver
 HDD_N@ : NO Hard Disc Redriver
 ODD@ : Optical Disc Drive
 TPC@ : Type-C function
 TPC_N@ : No Type-C function
 CNV@ : Intel WIFI
 CNV_N@ : NO Intel WIFI
 PBA@ : Finger Print on touch pad
 TPM@ : Trusted Platform Module
 TPM_N@ : No Trusted Platform Module
 KBL@ : Keyboard back light
 GS@ : G-Sensor function
 GS_N@ : No G-Sensor function
 HDMI_R@ : HDMI Redriver
 HDMI_N@ : No HDMI Redriver
 Debug@ : for Debug Card
 255@ : Codec 255
 256@ : Codec 256
 FOR15_17@ : Panel 15 or 17 inch
 FOR14@ : Panel 14 inch
 A3@ : 3cell & 2cell+ w/o BC1.2 + w/o Type-C
 A5@ : 4cell & 3cell + BC1.2 + Type-C

Power solution

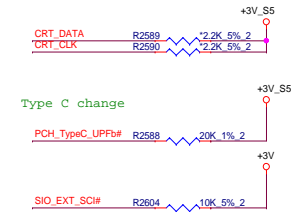
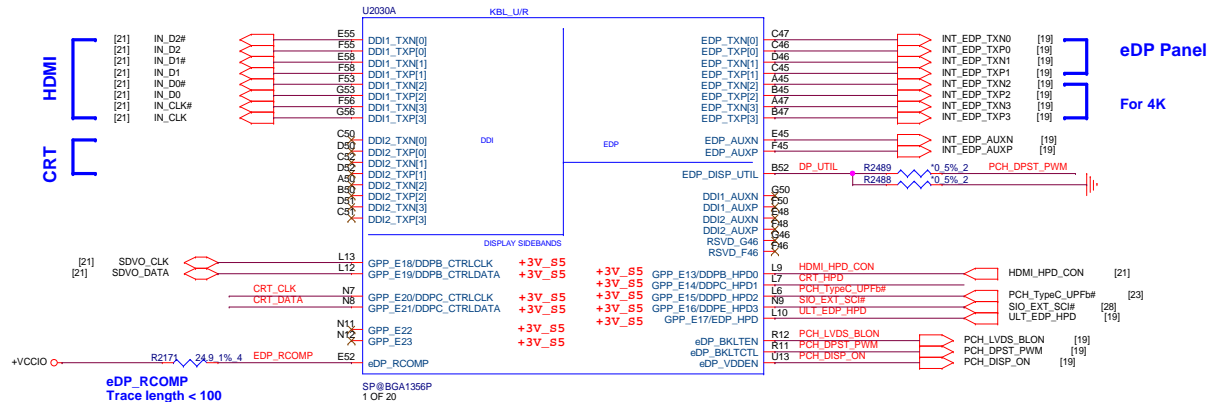


PCB 8L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : SVCC
 LAYER 6 : IN3
 LAYER 7 : SGND
 LAYER 8 : BOT

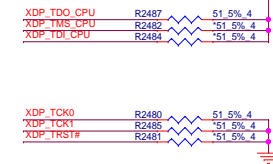
KabyLake ULT (DISPLAY,eDP)

Vinafix.com

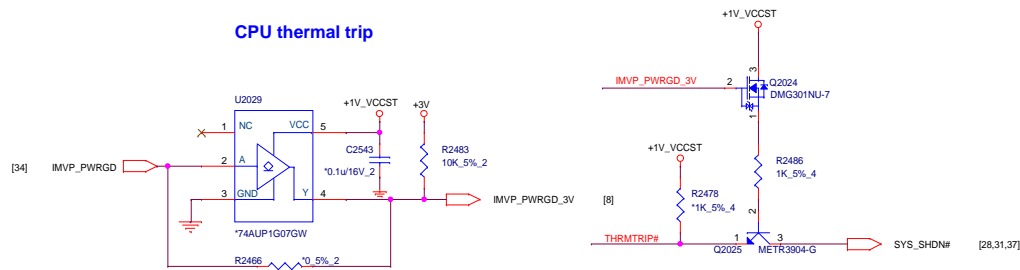


PCH JTAG
JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

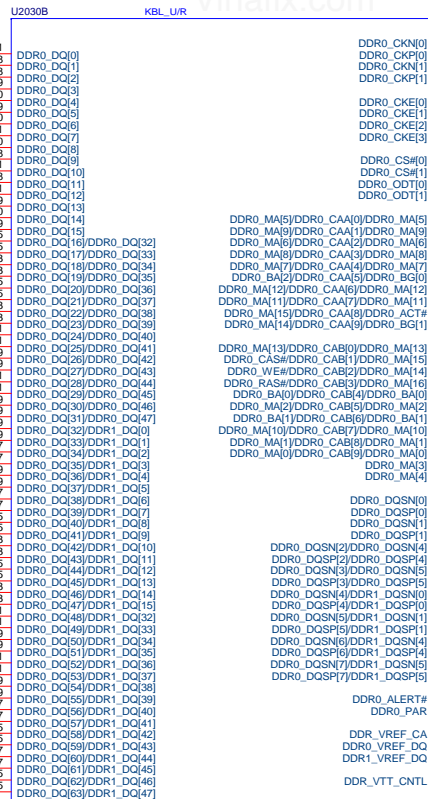
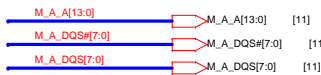


CPU thermal trip



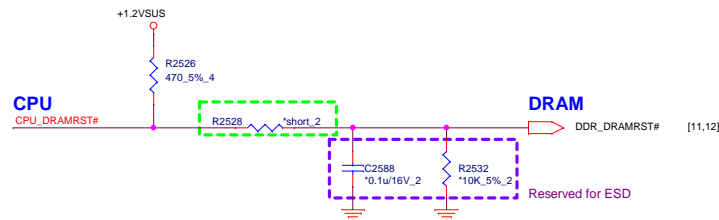
Change Data and DQS to interleave.

KabyLake ULT (DDR4)

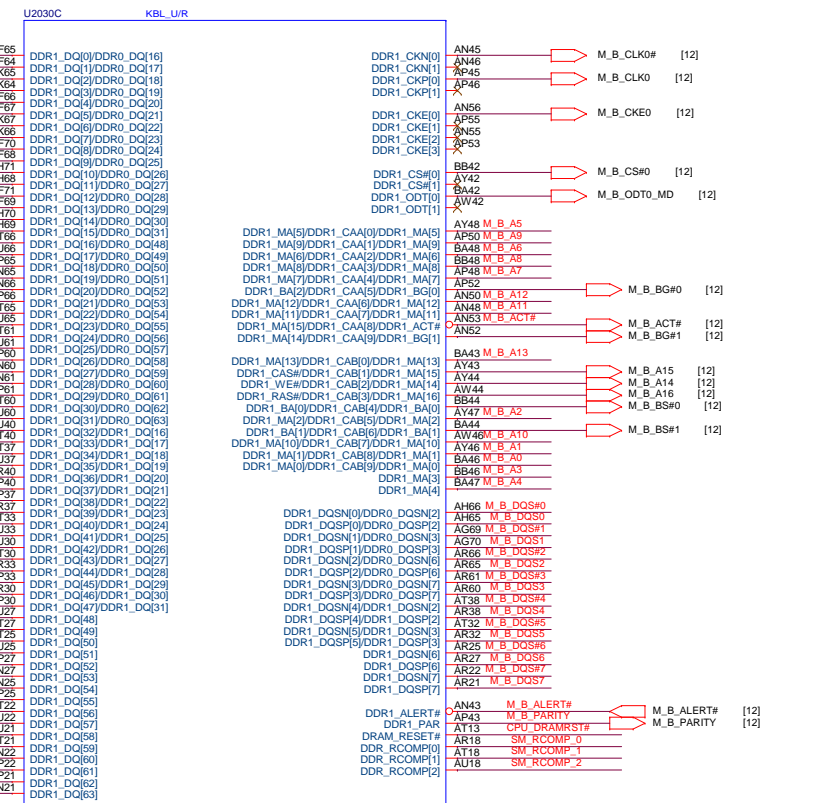
SP@BGA1356P
2 OF 20

Stuff Q54 for both UMA and GPU in DDR_VTT_CNTL

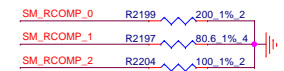
DRAMRST



KabyLake ULT (DDR4)

SP@BGA1356P
3 OF 20

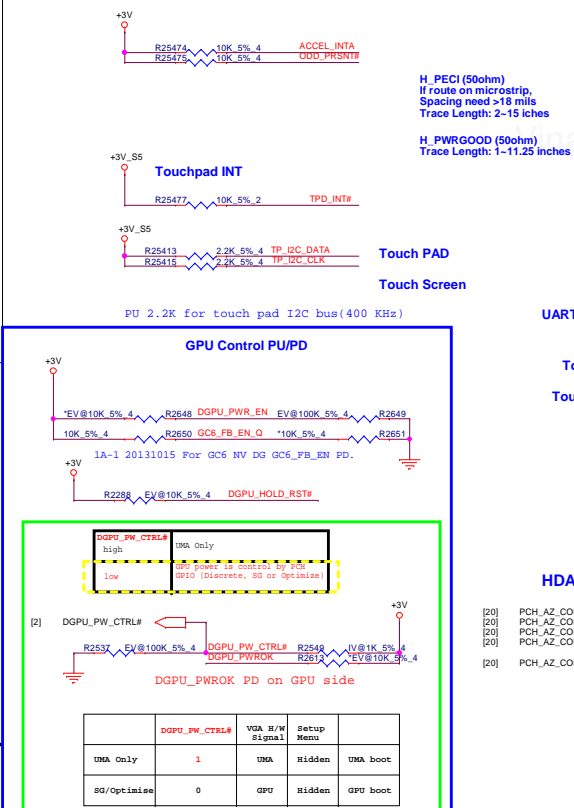
DRAM COMP



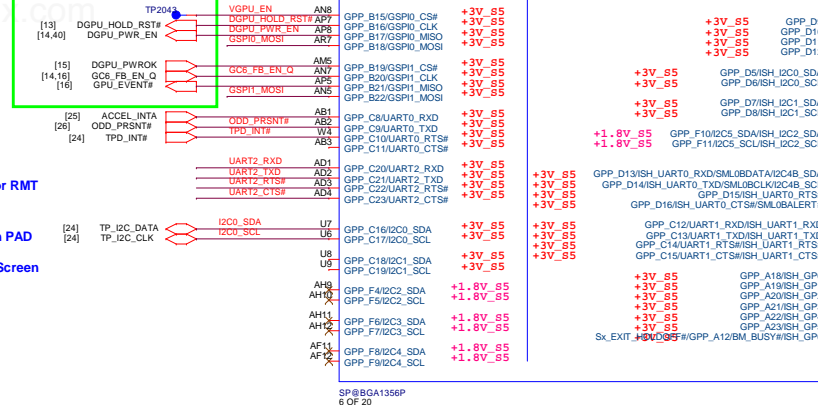
Quanta Computer Inc.

PROJECT : ZAU

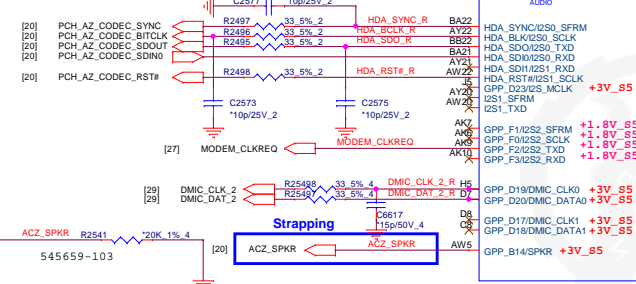
Size	Document Number	Rev
	KabyLake MEMORY	1A
Date:	Wednesday, April 10, 2019	Sheet 3 of 43



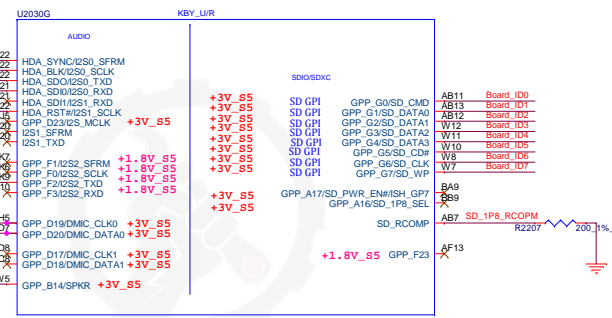
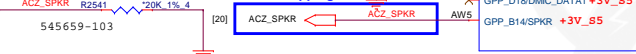
Add GPU Power Control Siganls



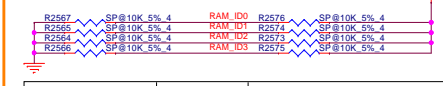
HDA



Strapping



RAM ID

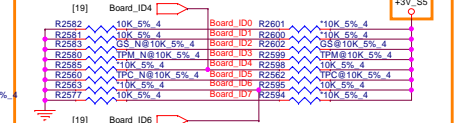


ID3	ID2	ID1	ID0	Vendor	Vendor PN	Quanta PN
0	0	0	0	Hynix 8Gb	HSAN8G6NCJR-VKC	AKD5QSG5TW13
0	0	0	1	Micron 8Gb	MT40A512M16L1Y-075:E	AKD5L2STL24
0	0	1	0	Micron 8Gb	MT40A512M16T8-062E:J	AKD5QSG5TL23
1	1	1	1	With out on board memory		

UART









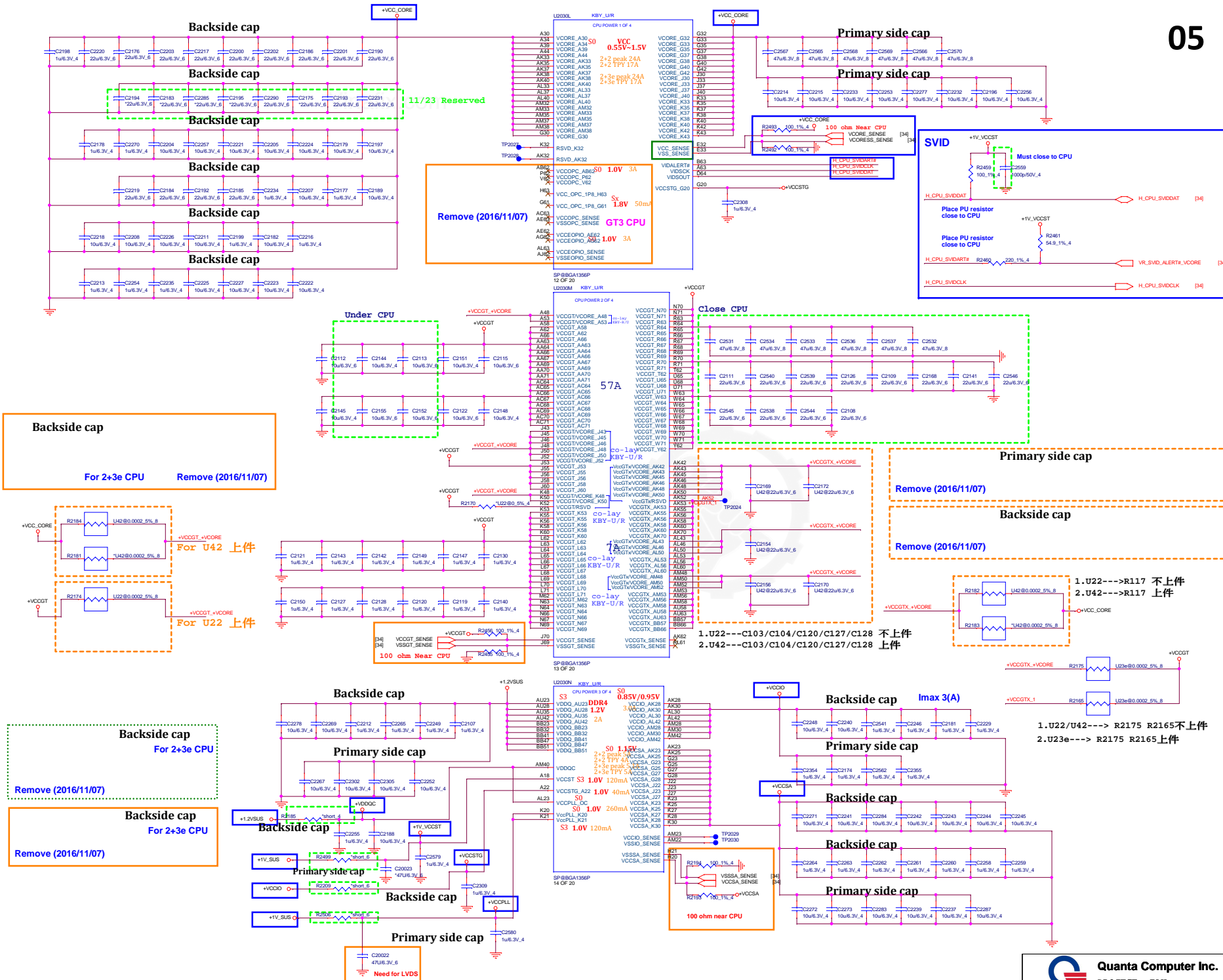
Board ID

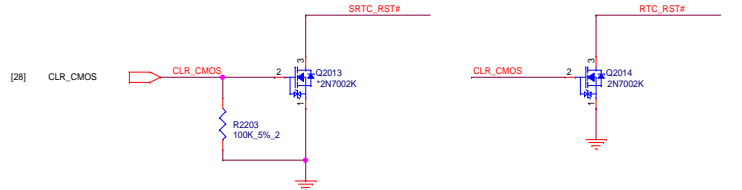
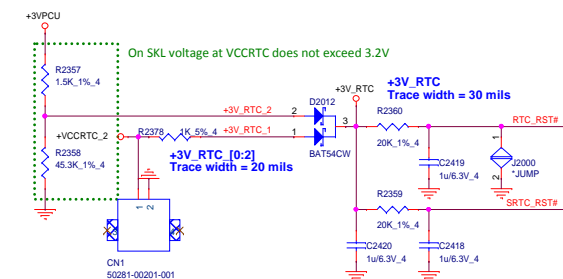
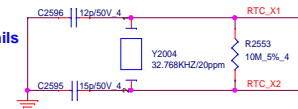
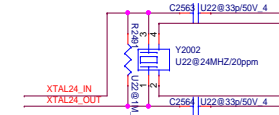
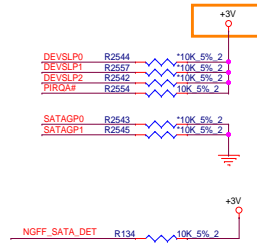
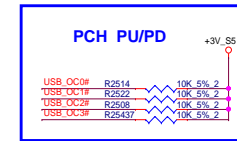


	Low	High
BOARD_ID0	Non eMMC	eMMC
BOARD_ID1	HDMI 1.4	HDMI2.0
BOARD_ID2	Non G-sensor(GS_N@)	G-sensor(GS@)
BOARD_ID3	Non TPM(TPM_N@)	TPM(TPM@)
BOARD_ID4	Non Touch panel	Touch panel (Control by Cable)
BOARD_ID5	Non Type-C(TPC_N@)	Type-C(TPC@)
BOARD_ID6	Single MIC(Cable control)	Dual MIC (DMIC@)
BOARD_ID7	Reserved (Default)	Reserve

Skylake-U Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V 
GPP_B18 (GSP10_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V 
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Crypt to TLS(iPD 20K) 1 = Enable Intel ME Crypt to TLS	+3V_S5 
GPP_B22 (GSP11_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V 
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	+3V_S5 
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 - 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 - 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 - 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 - 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal 
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	



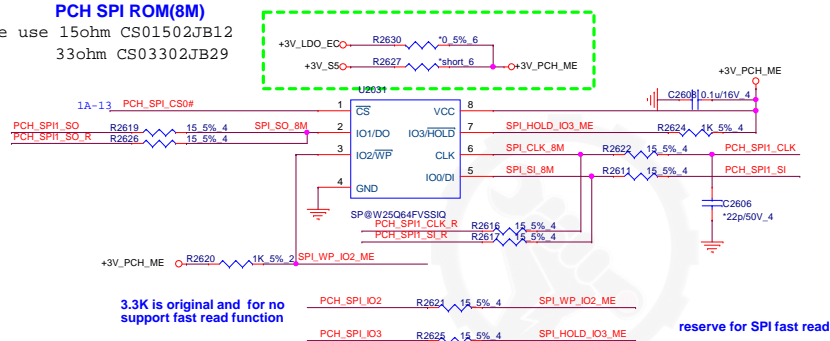
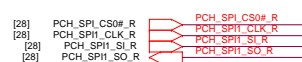




Termination Resistor Requirement for PCH PCHHOT# Pin
Reserve PU 150K resistor

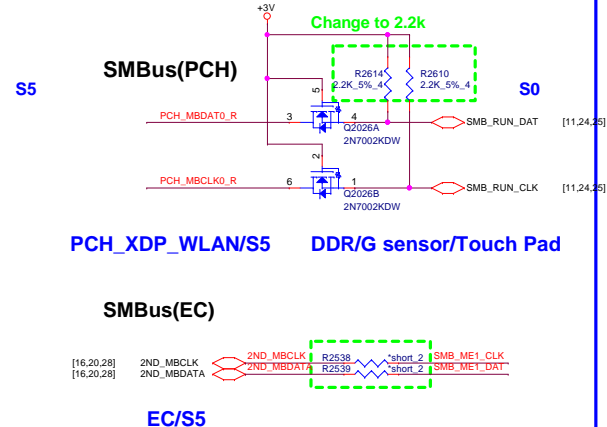
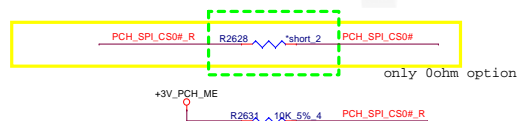
PCH SPI ROM(8M)

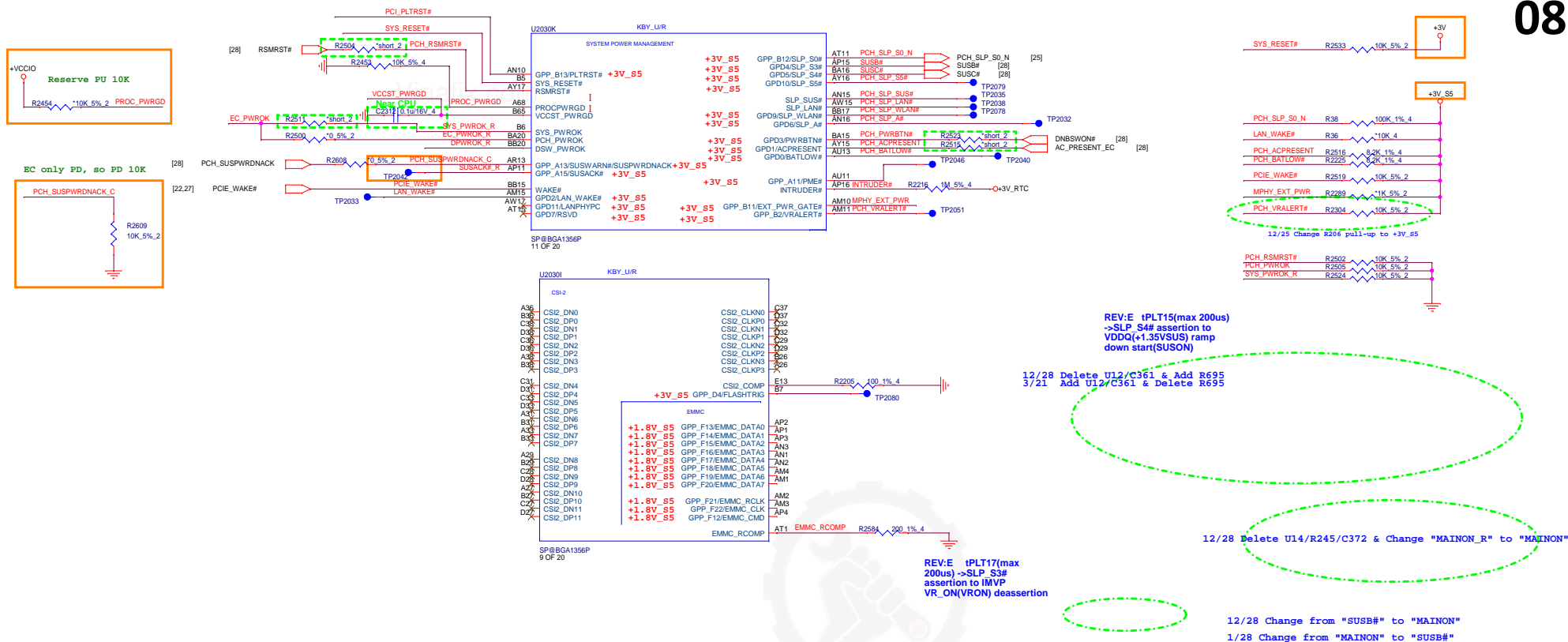
```
share use 15ohm CS01502JB12
          33ohm CS03302JB29
```



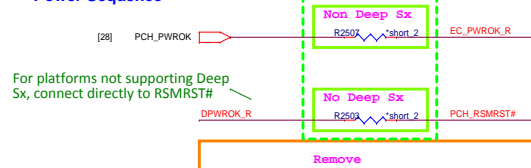
SP@ socket P/N: DG008000011 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Kabylake 3.3V	WND	8M	AKE3EZ-N001	W25Q64JVSSIQ
	GGD	8M	AKE2EZNOQ00	XD25B64CSIGR
	XMC	8M	AKE3EZPOX00	GM25QH64AAHIGT
Kabylake POA 3.3V	MXIC	1.6M	AKE3DZNOZ03	MX25L12873FSJ1-10G
	Winbond	1.6M	AKE3DF-KN01	W25Q128VSIQ
	GigaDevice	1.6M	AKE3DZNOQ02	GD25B127DSIGR

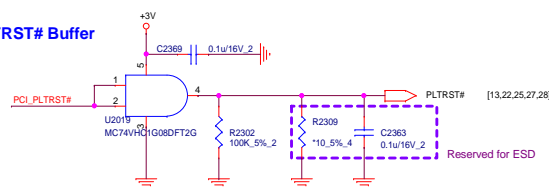




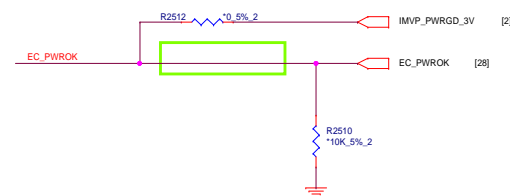
Power Sequence



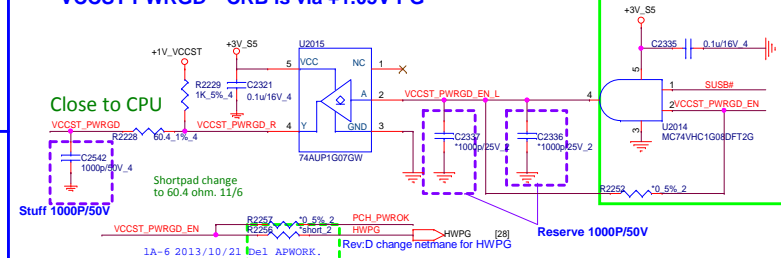
PLTRST# Buffer

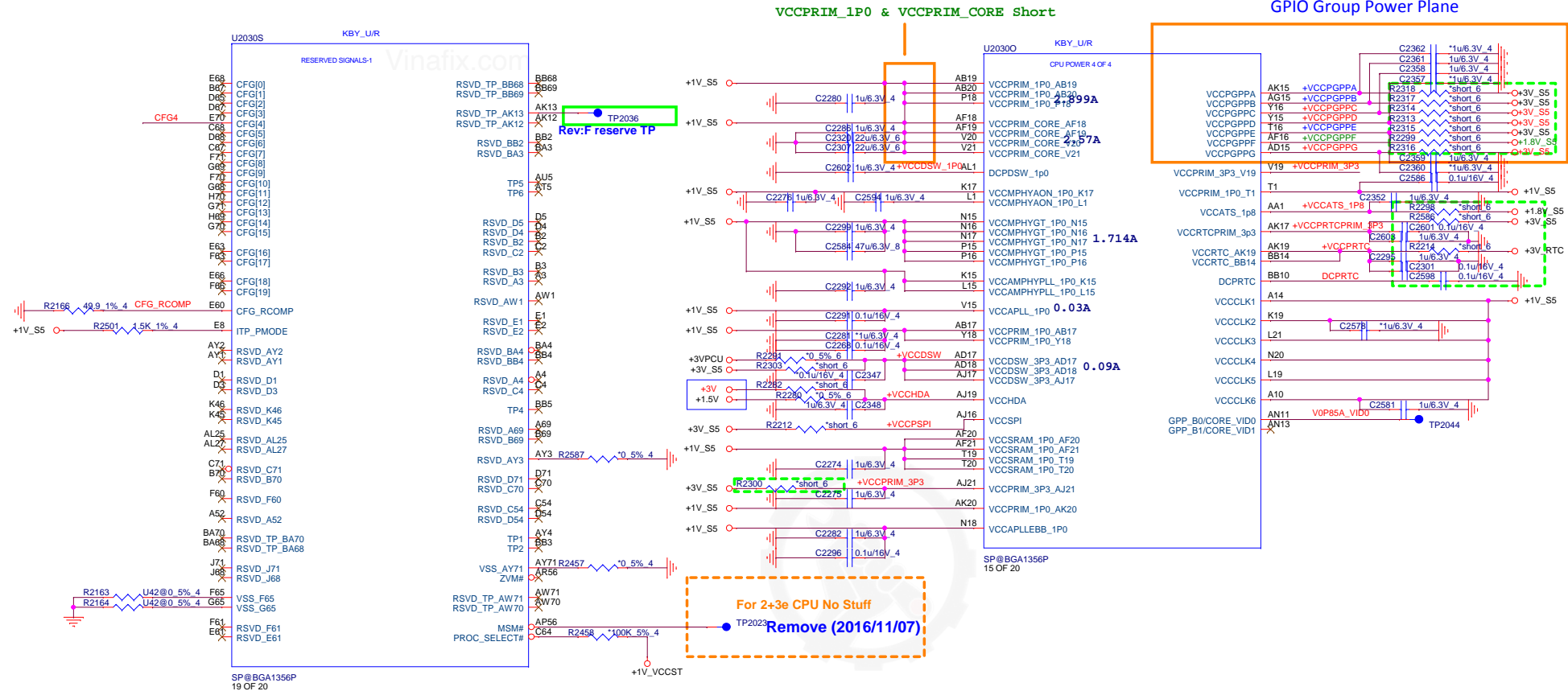


SYSPWOK



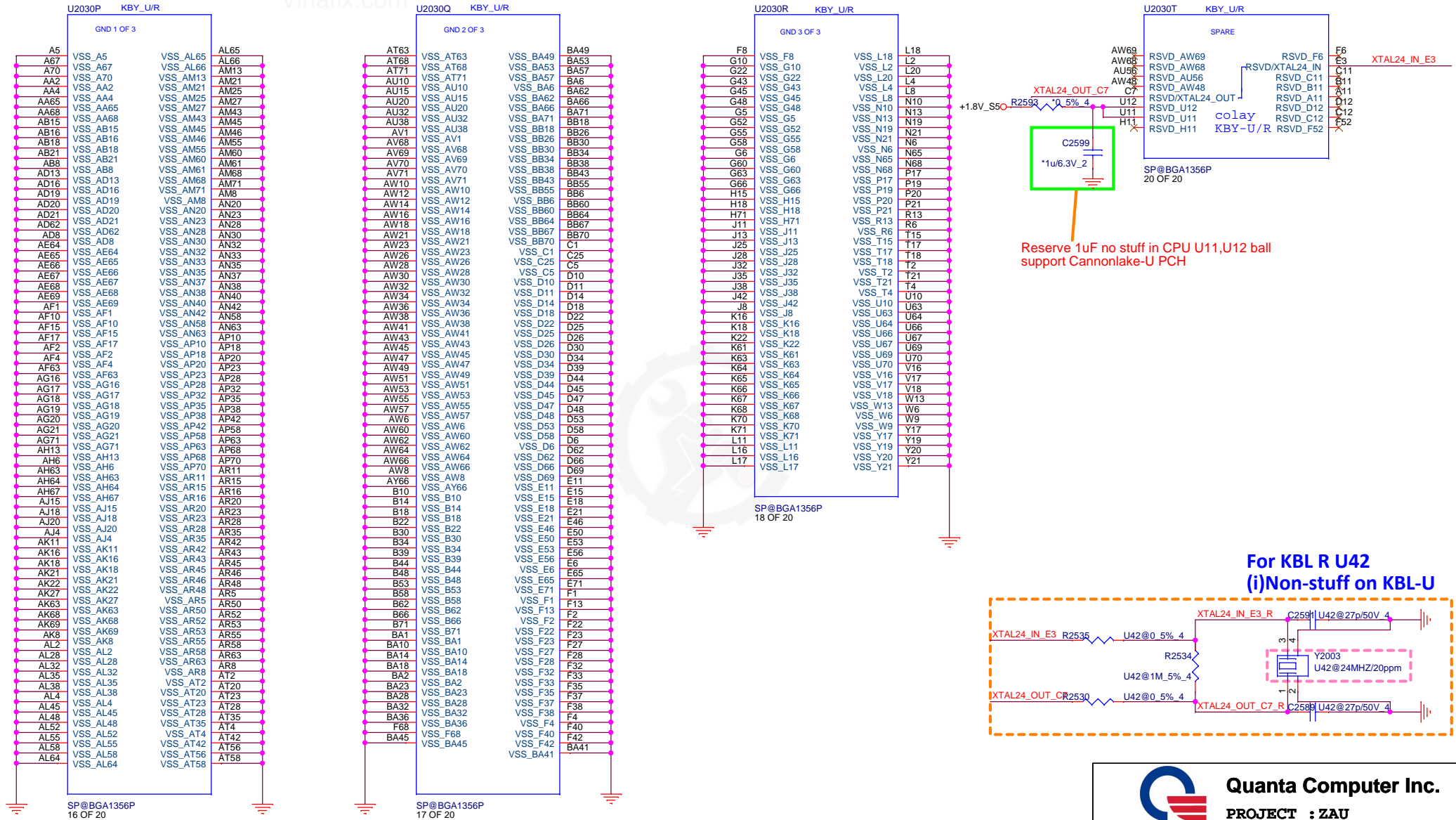
VCCST PWRGD CRB is via +1.05V PG

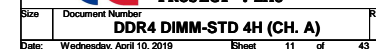


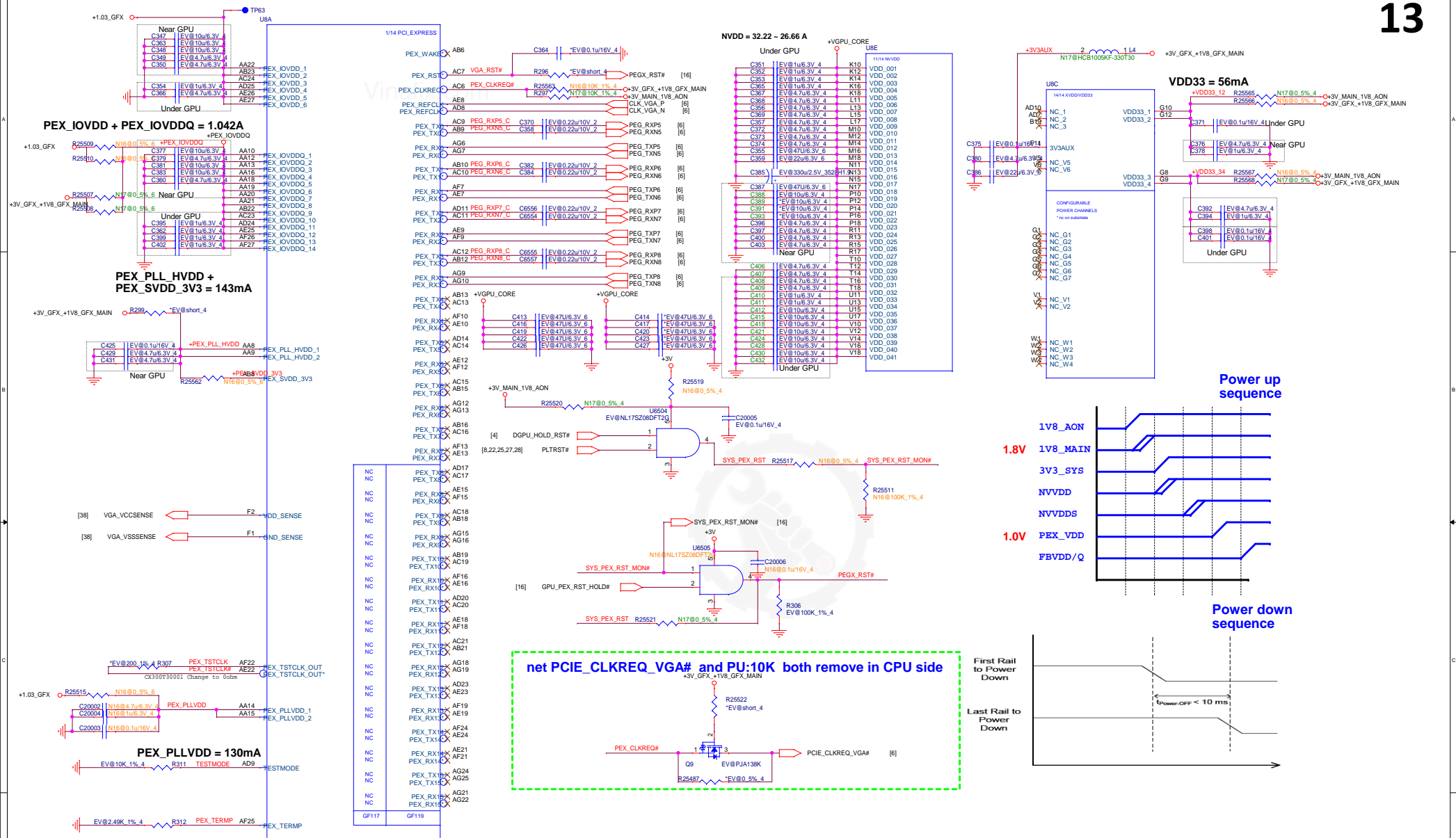


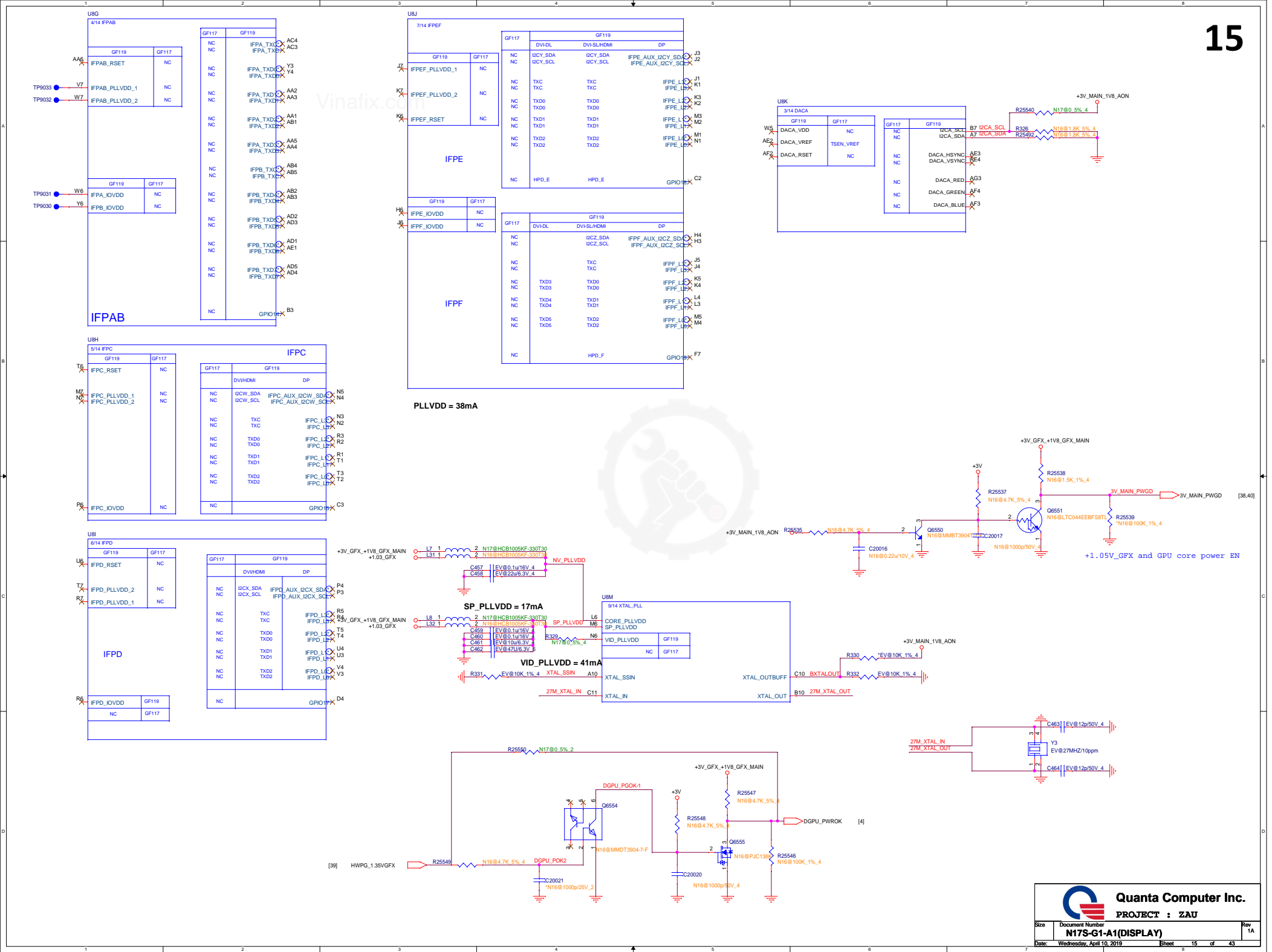
KabyLake ULT (GND)

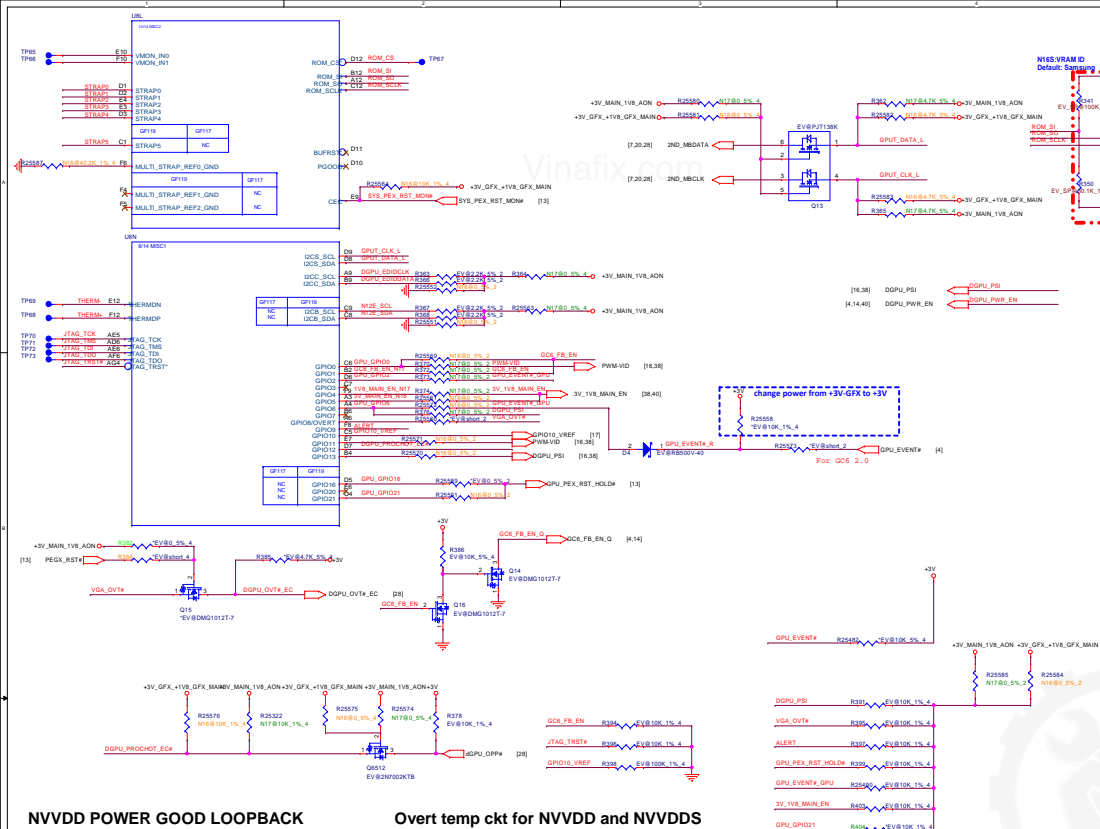
Vinafix.com





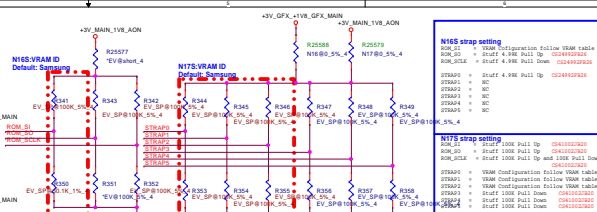






NVVDD POWER GOOD LOOPBACK

Overt temp ckt for NVVDD and NVVDDS



N16S GDDR5 Recommended Memories

RAM/C (2-B)	DESCRIPTION	Vendor	Vendor PN	QFN	ROM, SI (NIES VRAM IC)
0v0 (0000)	GD00S 256Mx32 3.2 GHz	Samsung B die	K4G80 325FB-BH-C28	AKG5QG0DT518	Rpu(R241) No staff Rpu(R250) 4.99K (C32492F2B26)
0v8 (1000)	GD00S 256Mx32 3 GHz	Micron B die	MT51J27326K32EF-70-B	AKG5Q0UTL32	Rpu(R241) 4.99K (C32492F2B26) Rpu(R250) No staff
0v9 (1001)	GD00S 256Mx32 3 GHz	Hynix A die	JS50C8244JR-C	AKG5Q0UTW26	Rpu(R241) 10K (C31302J0B28) Rpu(R250) No staff

RAM, SI Resistor(VRAM IC)	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99K (C32492F2B26)	1000	0000
10K (C31002J0B28)	1001	0001
15K (C31502F2B24)	0010	0010
20K (C32002F2B29)	1011	0011
24.9K (C32492F2B16)	1100	0100
30.1K (C33012F2B18)	0101	0101
34.8K (shortage)	1110	0110
45.3K (C3452F2B18)	1111	0111

ROM, SO	
Rpu(R343)	4.99K (C32492F2B26)
Rpd(R351)	No staff

ROM, SCLK	
Rpu(R342)	No staff
Rpd(R352)	4.99K (C32492F2B26)

STRAP5	
Rpu(R348)	No staff
Rpd(R358)	No staff

STRAP4	
Rpu(R347)	No staff
Rpd(R357)	No staff

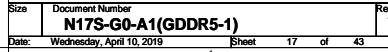
N17S-G0/G2 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor PN	QFN	ROM_Si
0x0	GD0R5 256Mx32 7 GHz	Samsung B die	K4G80325FB-RC28	AKG5SQGDT518	Rpu(R34F) 100K (C#41002J020)
0x4	GD0R5 256Mx32 7 GHz	Micron B die	MT512526M32HF-70:B18	AKG5SQGUTL32	
0x5	GD0R5 256Mx32 7 GHz	Hynix A die	H5G0CB824AJR-ROC	AKG5SQGUTW26	Rpd(R350) No staff

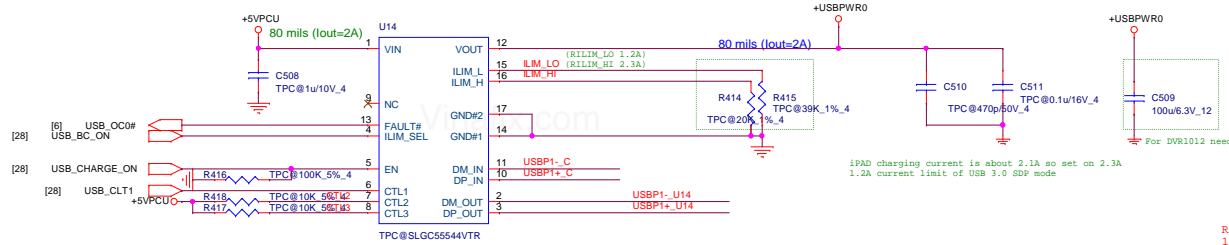
	STRAP2	STRAP1	STRAP0	
Samsung	L	L	L	0x0
Micron	H	L	L	0x4
Hynix	H	L	H	0x5

		Samsung	Micron	Hynix
STRAP2	Rpu(R346)		100K (CS41002/B20)	100K (CS41002/B20)
	Rpu(R355)	100K (CS41002/B20)		
STRAP1	Rpu(R345)			
	Rpu(R354)	100K (CS41002/B20)	100K (CS41002/B20)	100K (CS41002/B20)
STRAP0	Rpu(R354)			
	Rpu(R344)	100K (CS41002/B20)	100K (CS41002/B20)	100K (CS41002/B20)
STRAP0	Rpu(R344)			100K (CS41002/B20)
	Rpu(R353)	100K (CS41002/B20)	100K (CS41002/B20)	

ROM_S0	
Rpu(R343)	100K (CS41002,JB20)
Rpd(R351)	No staff
ROM_S0L_K	
Rpu(R342)	100K (CS41002,JB20)
Rpd(R352)	100K (CS41002,JB20)
STRAP5	
Rpu(R349)	No staff
Rpd(R358)	100K (CS41002,JB20)
STRAP4	
Rpu(R348)	No staff
Rpd(R357)	100K (CS41002,JB20)
STRAP3	
Rpu(R347)	No staff
Rpd(R356)	100K (CS41002,JB20)



USB Charger to 3.0 (UBC)

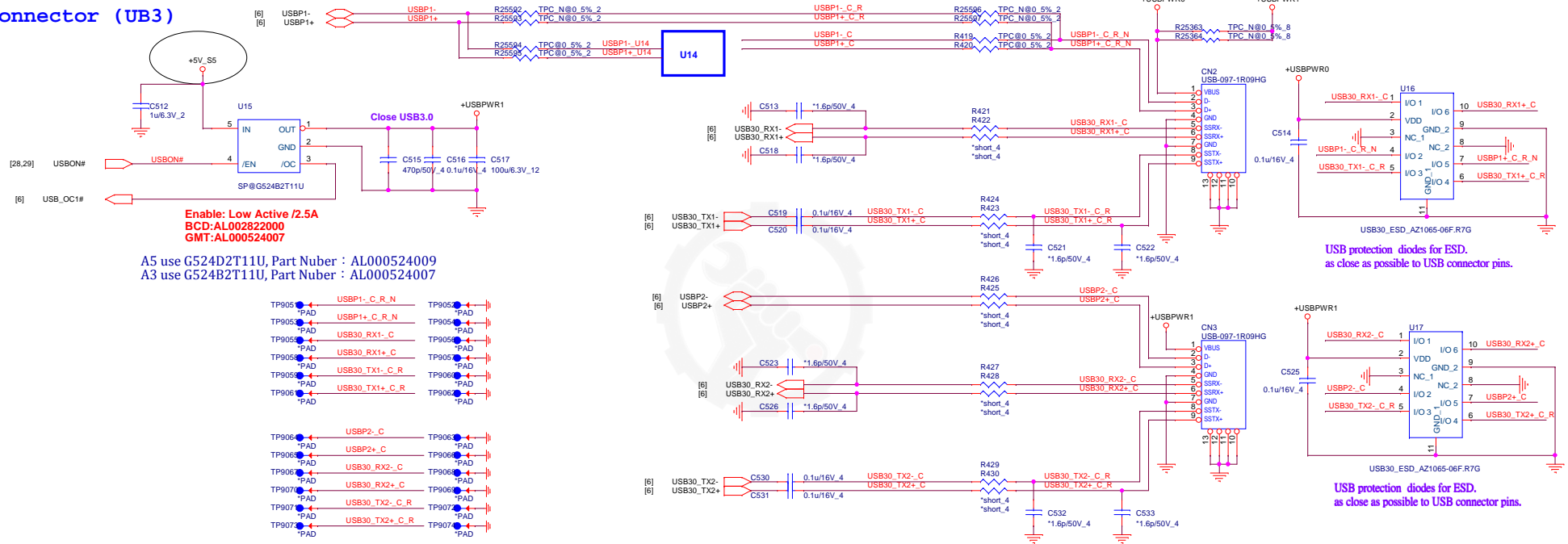


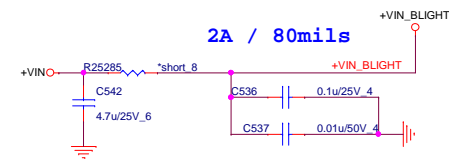
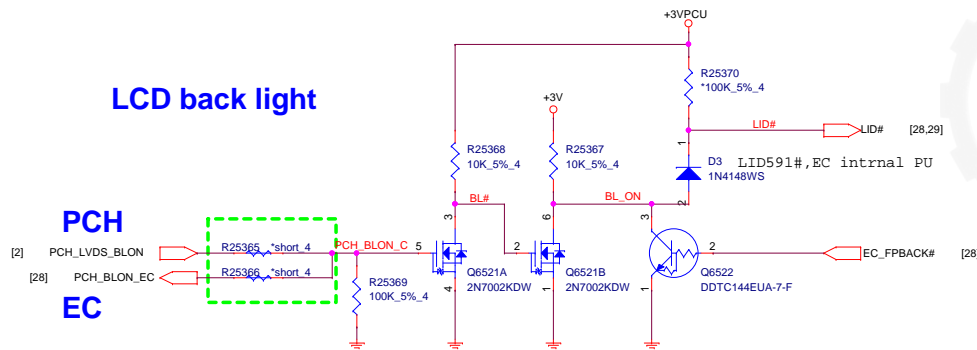
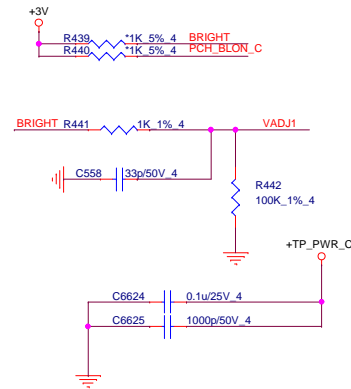
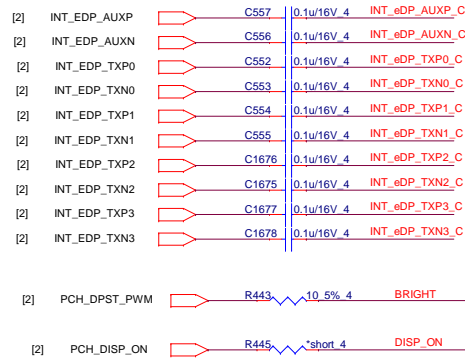
TI: AL002544001 (TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

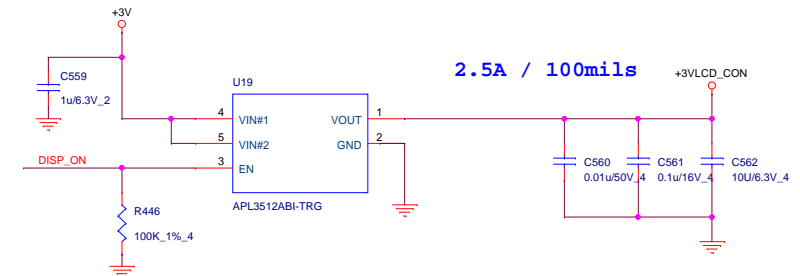
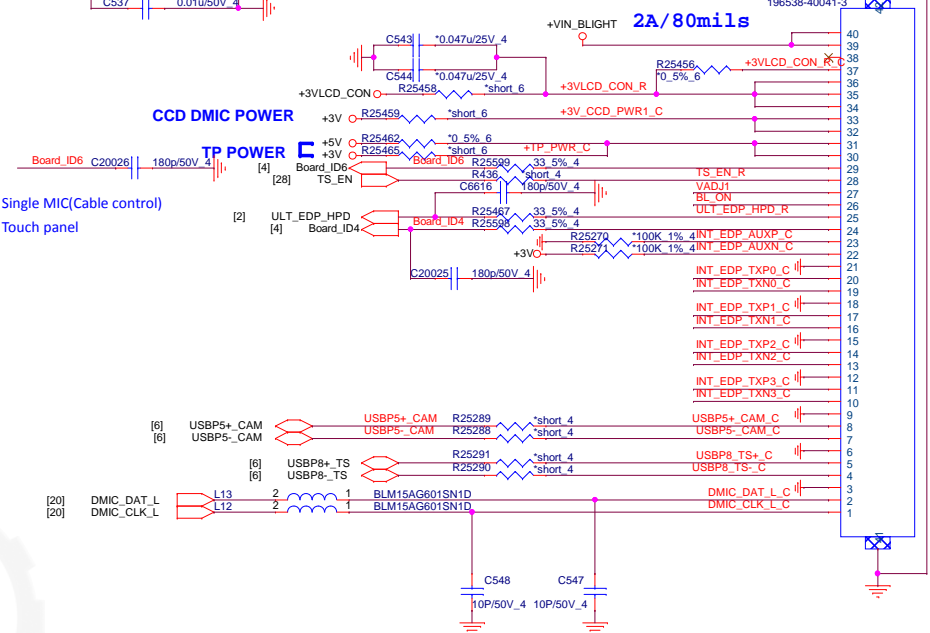
$$IOS_typ(mA) = 50,250 / \{RILIM_XX(k\Omega) + 0.1\}$$

USB 3.0 Connector (UB3)

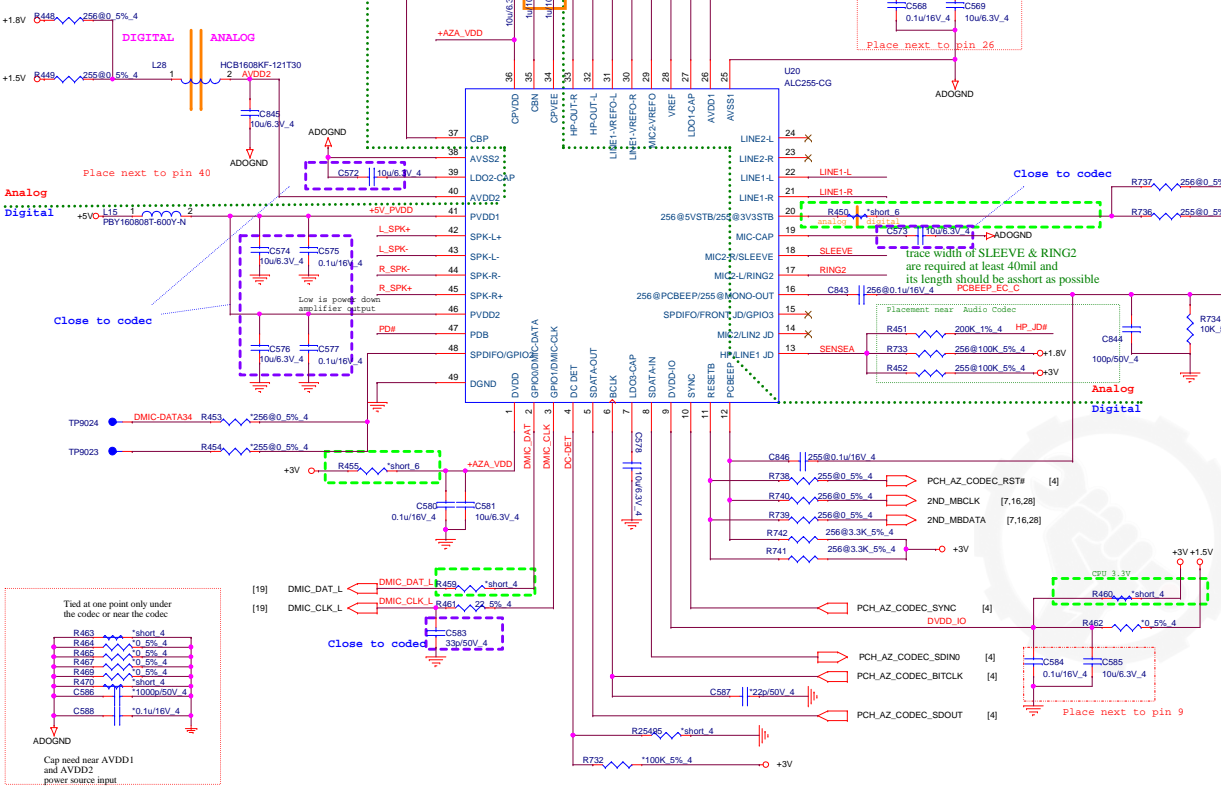




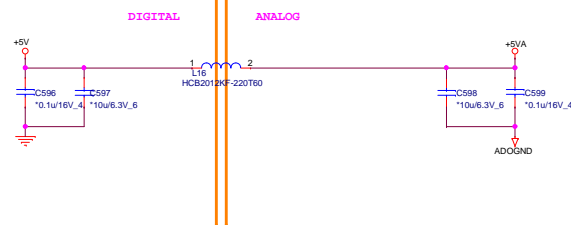
eDP Conn.



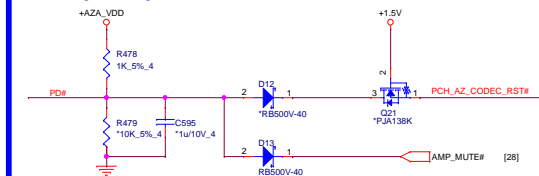
Codec PWR 1.5V(ADO)



Codec PWR 5V(ADO)

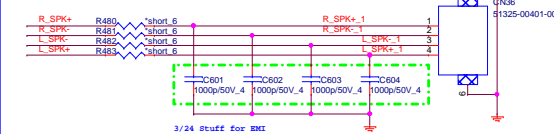


Mute(ADO)



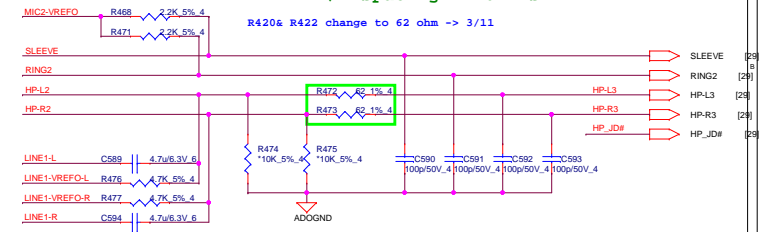
Internal Speaker

4 ohm : 40mil for each signal
40mil for each signal



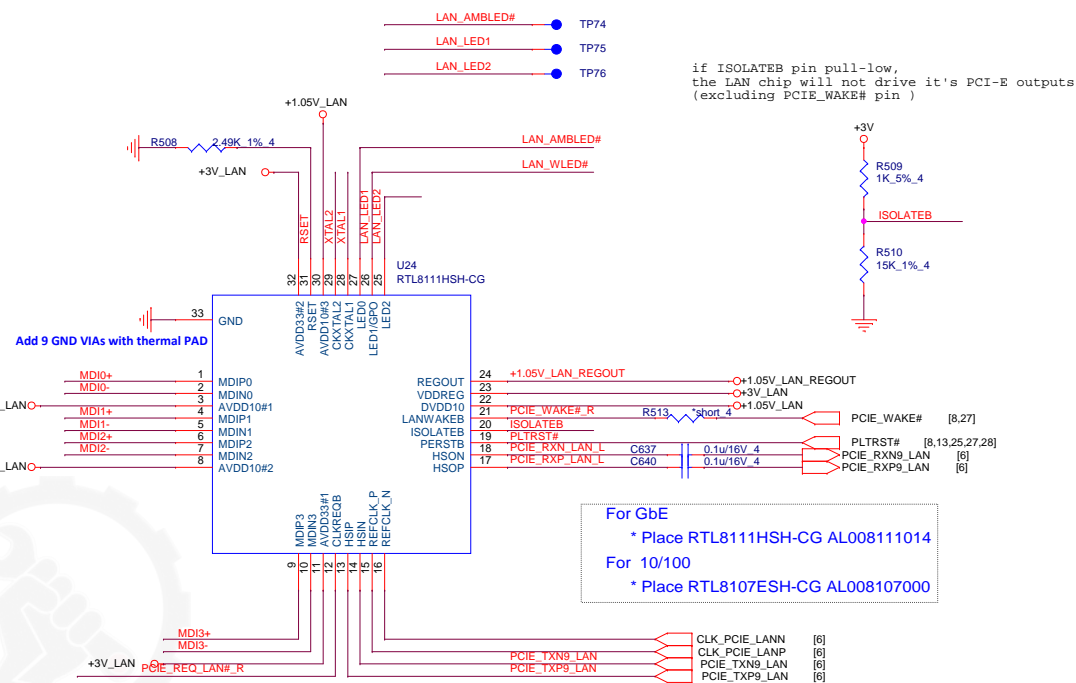
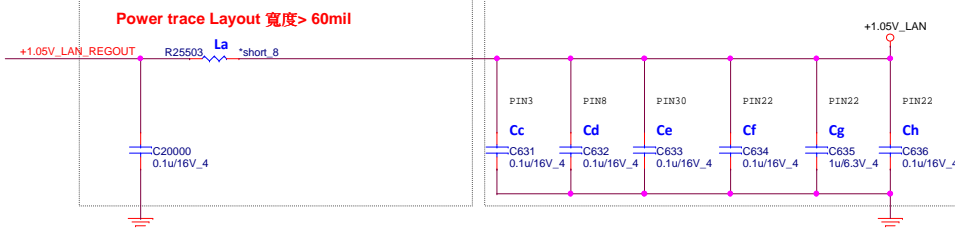
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils



* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 22(reserved)



Ub

U25

MDI2+ 2 MDI2- 1

MDI3+ 3 MDI3- 2

MDI0+ 4 MDI0- 3

MDI1+ 5 MDI1- 4

TD1+ 6 TD1- 5

TD2+ 7 TD2- 6

TD3+ 8 TD3- 7

TD4+ 9 TD4- 8

MX1+ 10 MX1- 9

MX2+ 11 MX2- 10

MX3+ 12 MX3- 11

MX4+ 13 MX4- 12

MDI2+ 1 MDI2- 1

MDI3+ 2 MDI3- 2

MDI0+ 3 MDI0- 3

MDI1+ 4 MDI1- 4

LAN_MCTG0 21 LAN_MCTG1 22 LAN_MCTG2 23 LAN_MCTG3 24

NS892407 25

GND 26

TRA_V_DAC 1

TRB_V_DAC 2

TRC_V_DAC 3

TRD_V_DAC 4

TCT1 5

TCT2 6

TCT3 7

TCT4 8

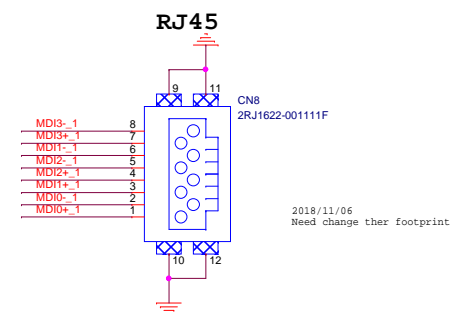
GND 9

C645 0.01uF 50V_4

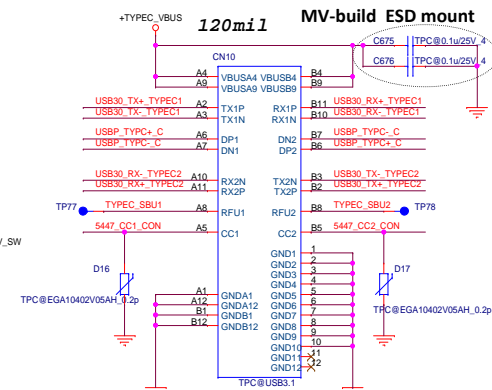
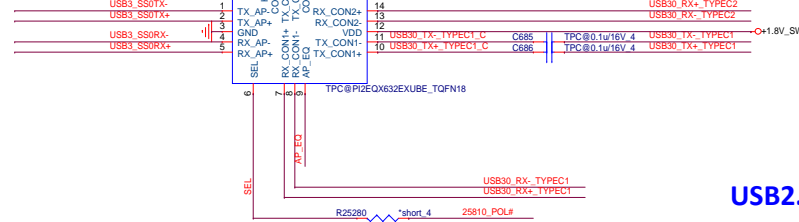
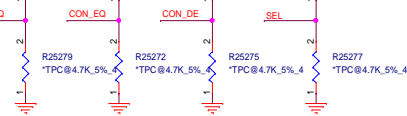
C646 10p3KV_1808

For 10/100 : Ra,Rb

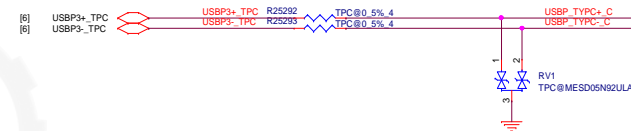
For Giga : Ra,Rb,Rc,Rd



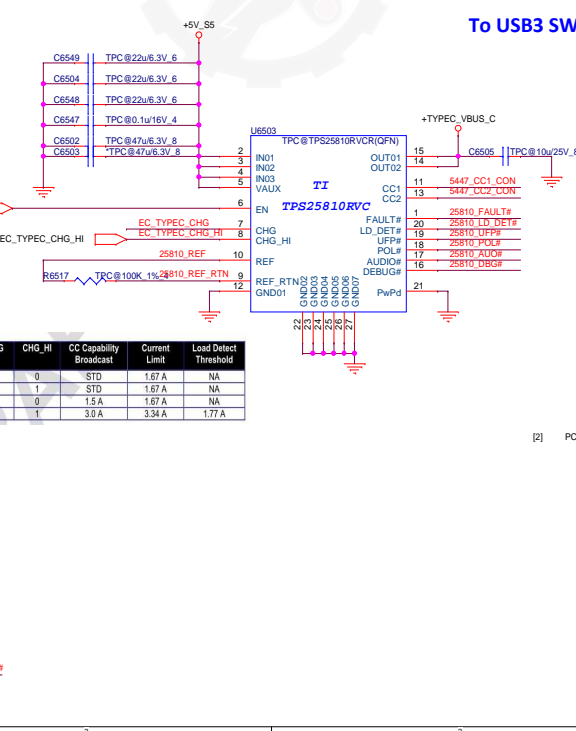
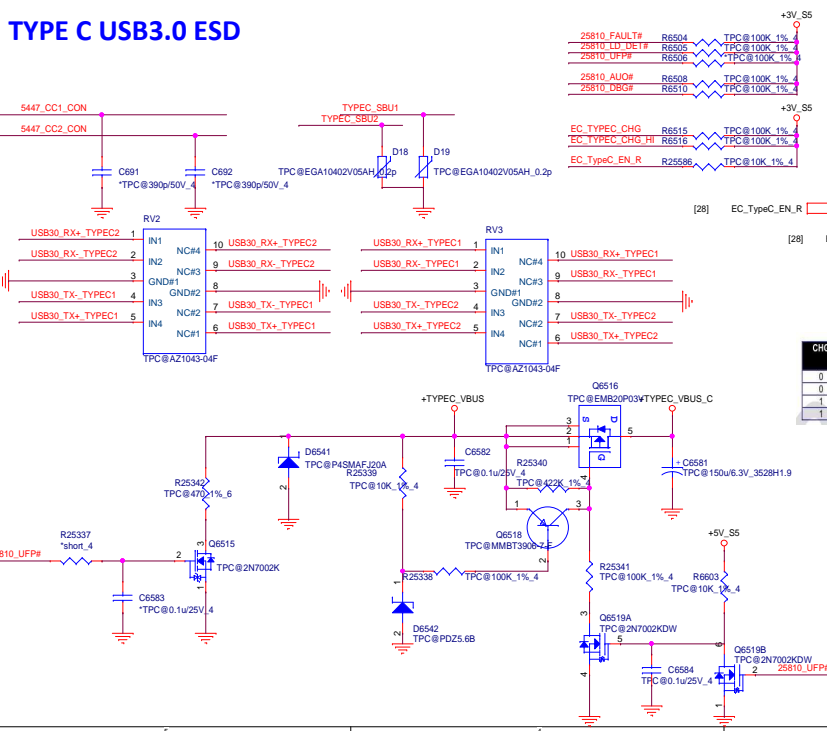
TYPE C and MUX PI2EQX632EXUBE



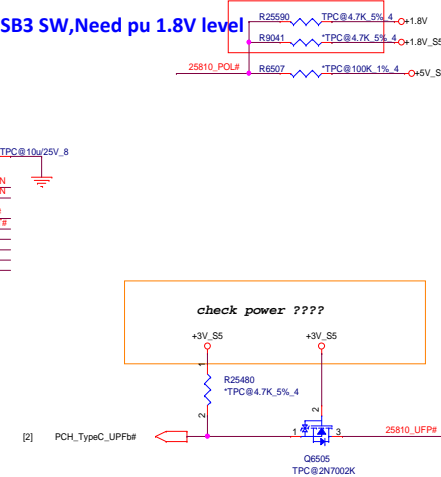
USB2.0



TYPE C USB3.0 ESD



To USB3 SW,Need pu 1.8V level

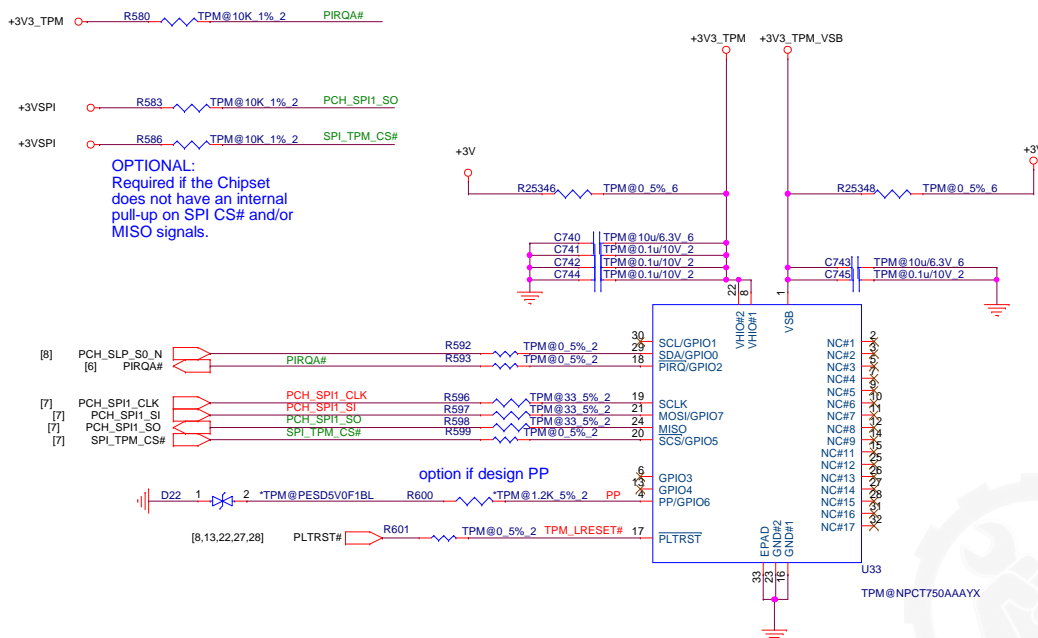


[illegible]

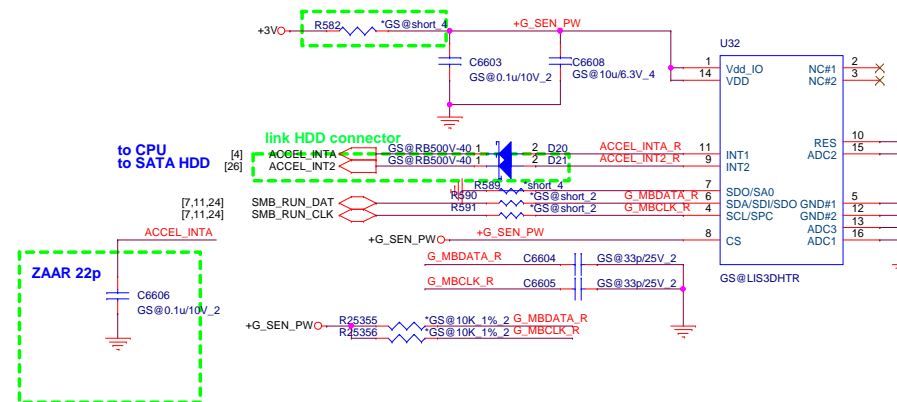
The schematic shows the internal wiring of the FAN3041-00 module. It includes four voltage regulators: two +3V regulators (R576, R25372) and two +5V regulators (R25373, R575). The +5V regulator R575 is labeled '*short_8'. A MOSFET Q6523 (METR3904-G) is used as a switch. The input signal FAN_PWM is connected to pin 1 of the MOSFET. The output of the MOSFET is connected to the FAN3041-00 module via a 30mil trace. The module has pins labeled FAN3 50278-00401-00. The module also has a connection to ground.

[illegible]

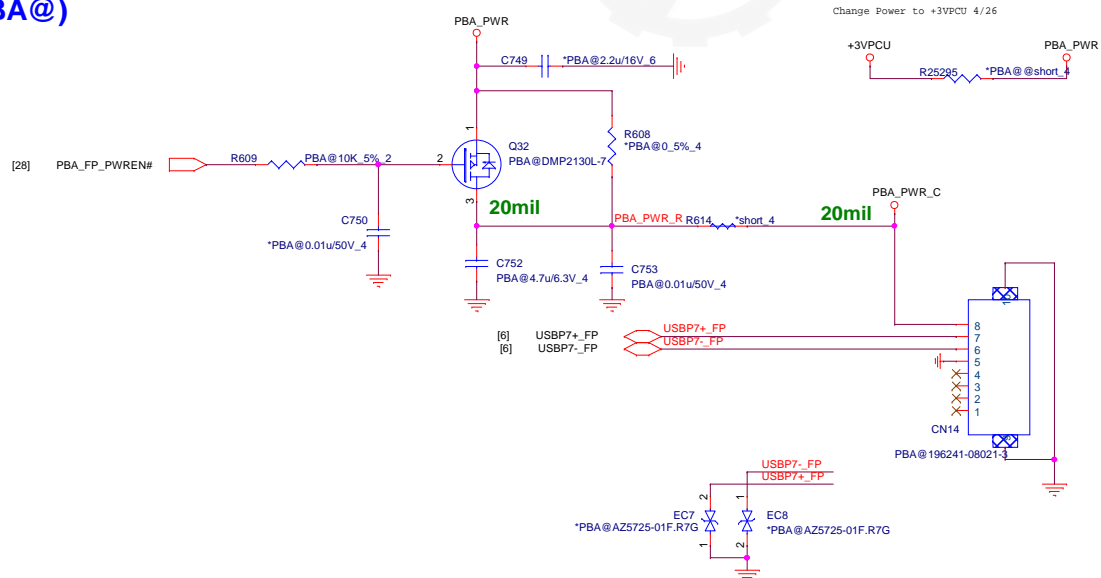
TPM NPCT750



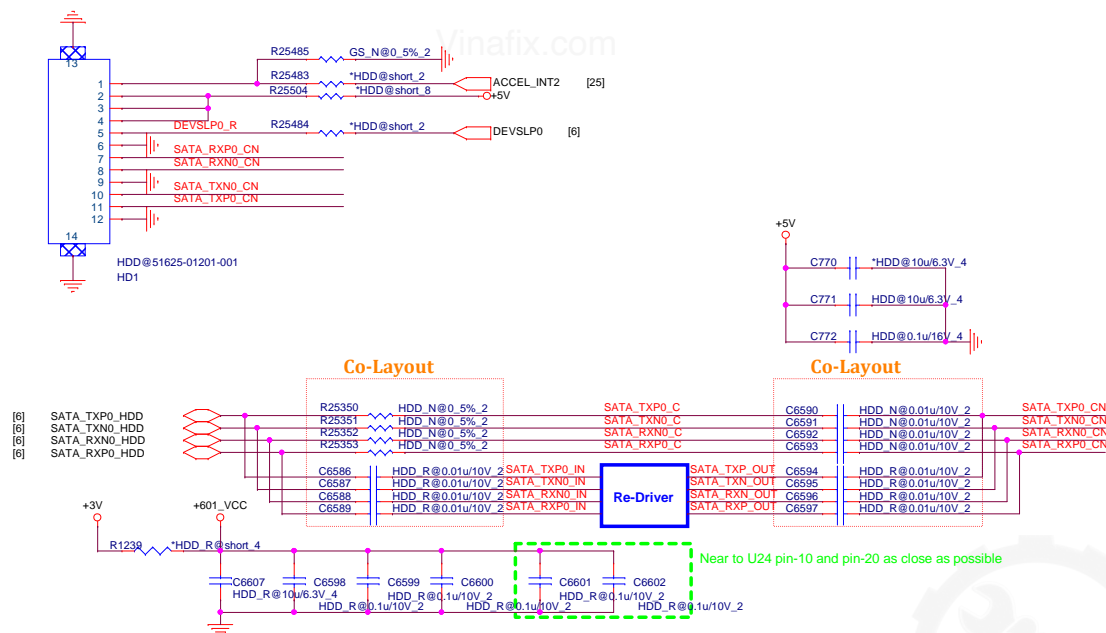
G-sensor (GS@)



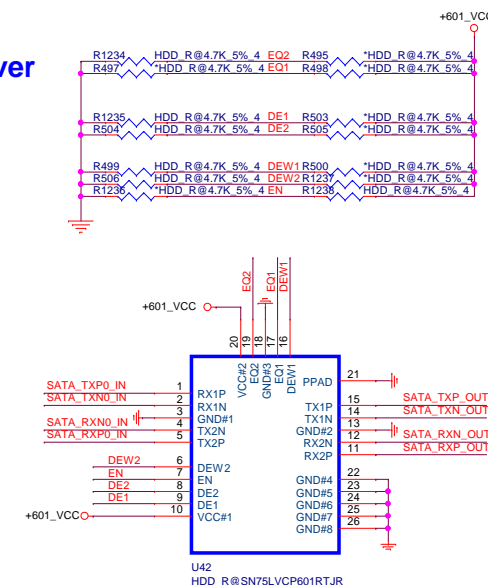
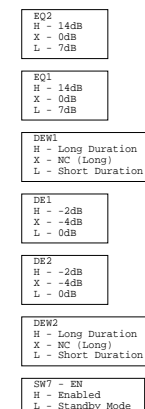
PBA (PBA@)



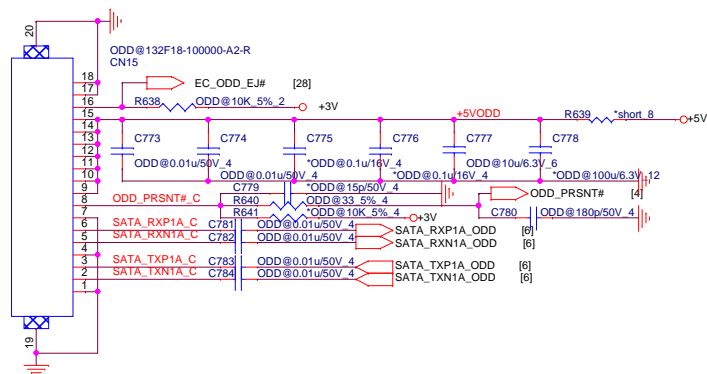
SATA HDD & LED



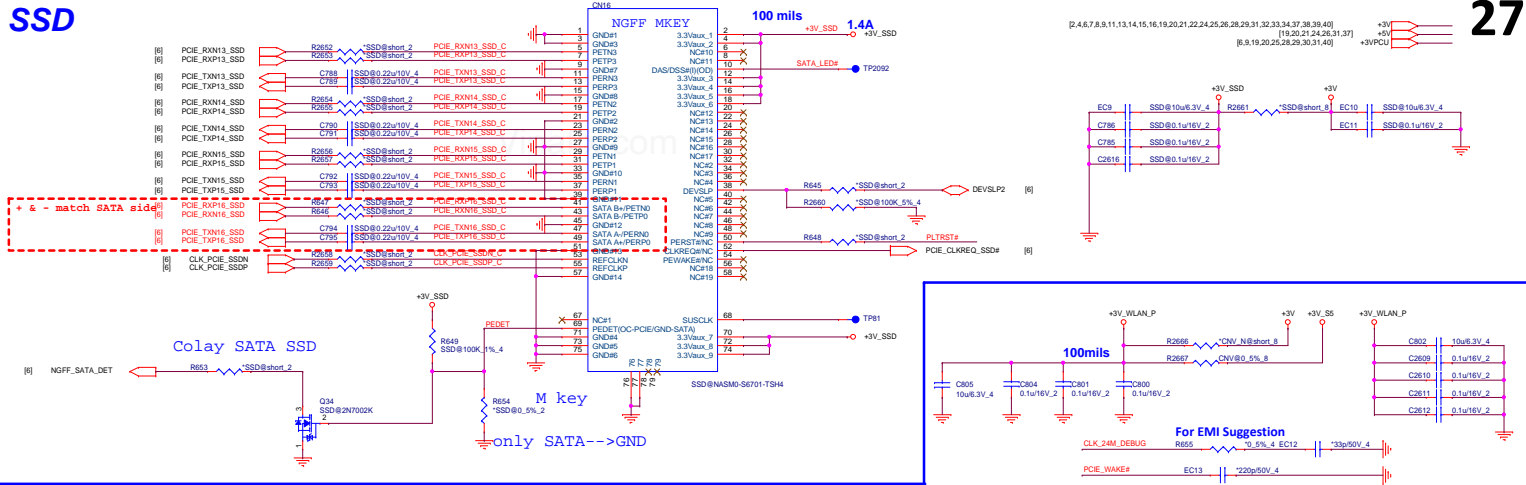
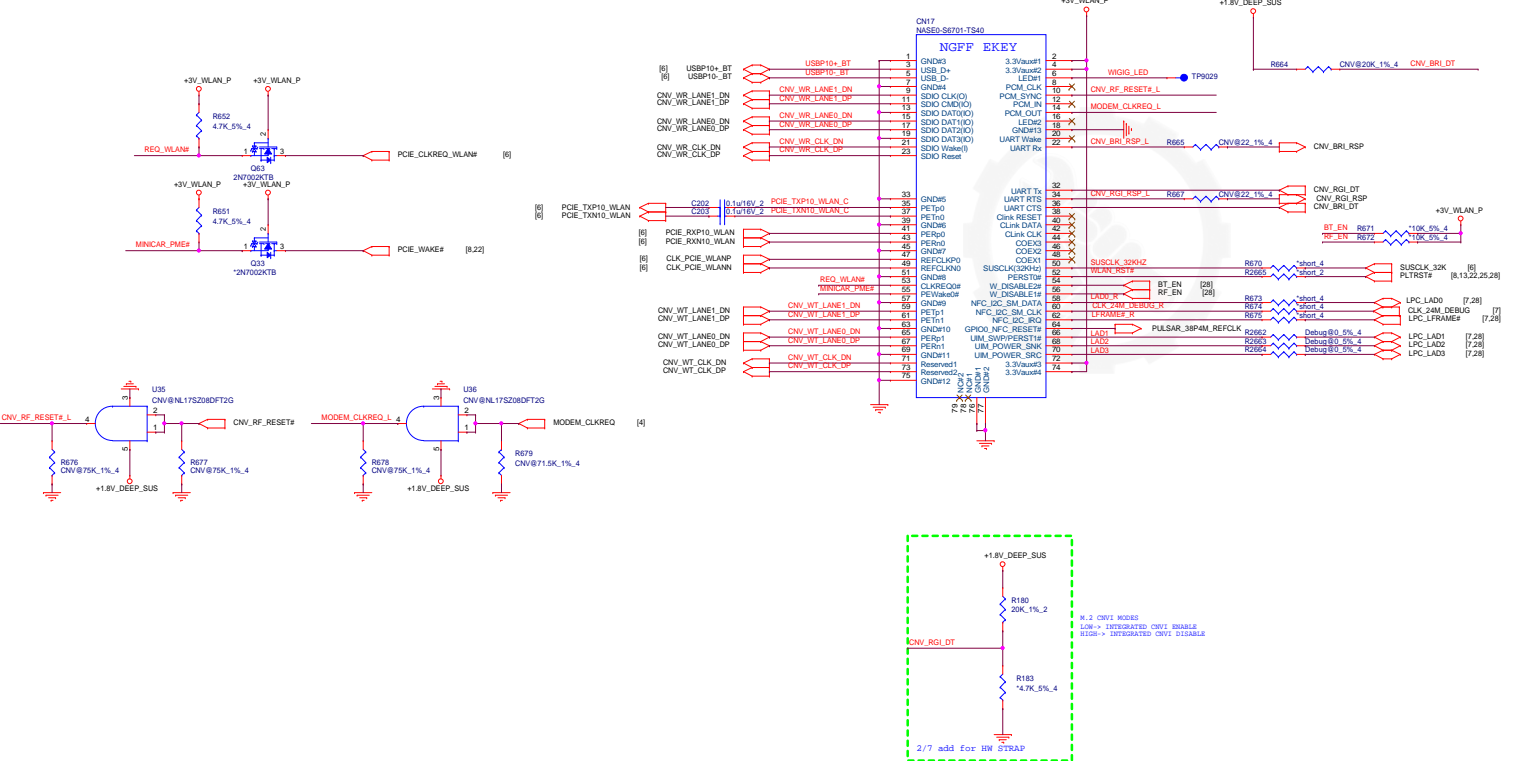
SATA HDD Re-driver



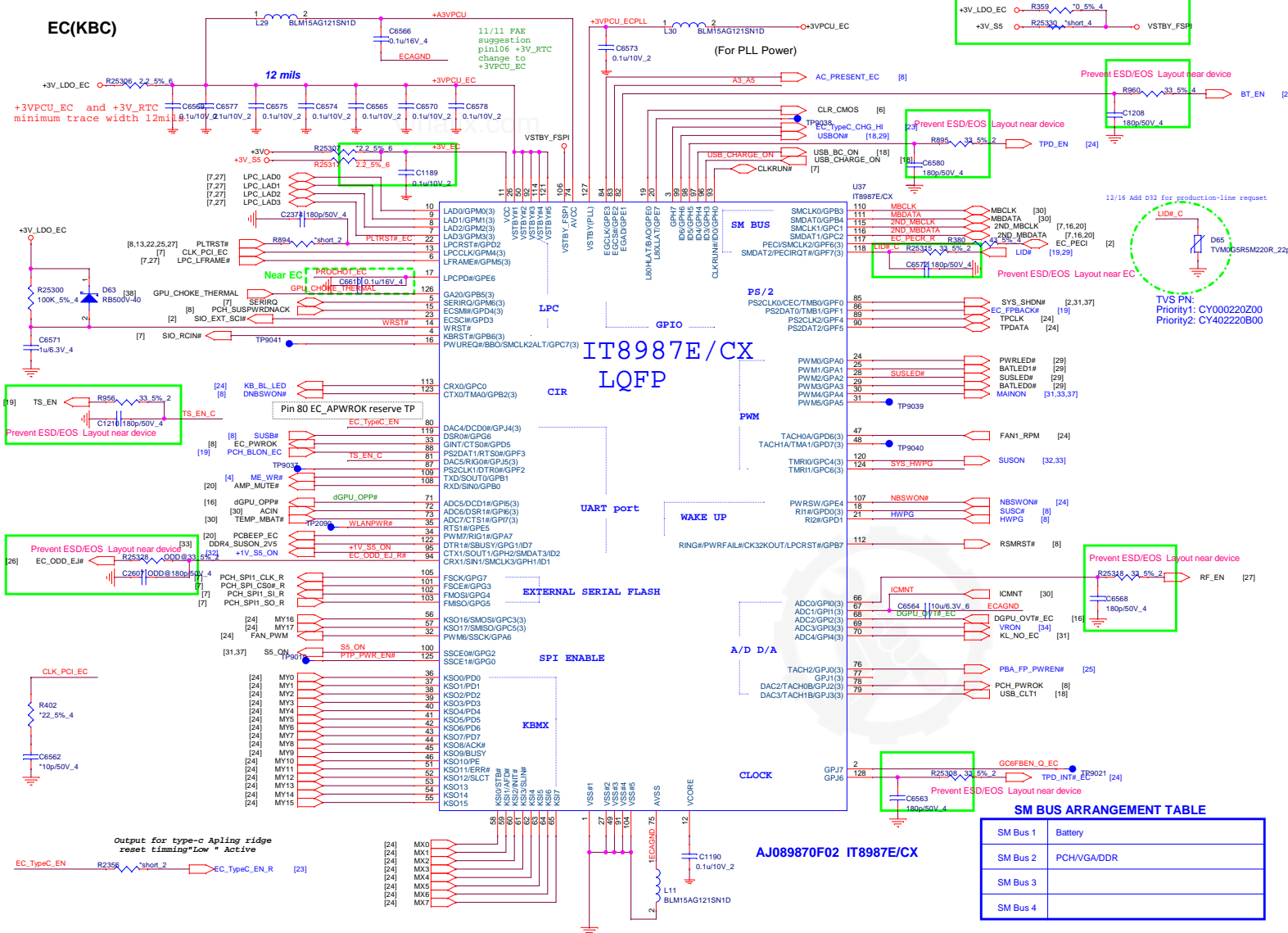
SATA ODD (ODD@)



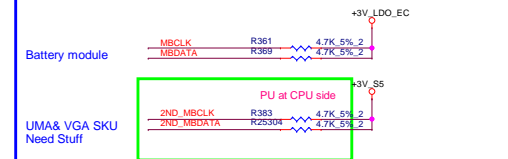
SSD

**WLAN**

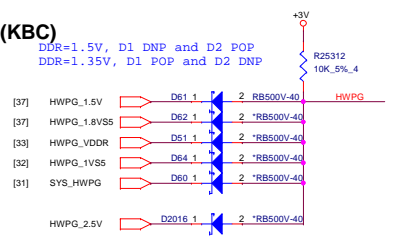
EC(KBC)



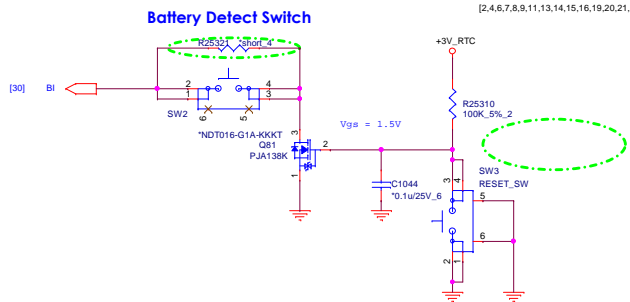
SM BUS PU(KBC)



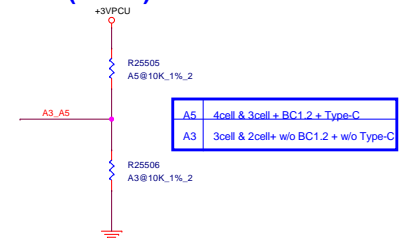
HWPG(KBC)



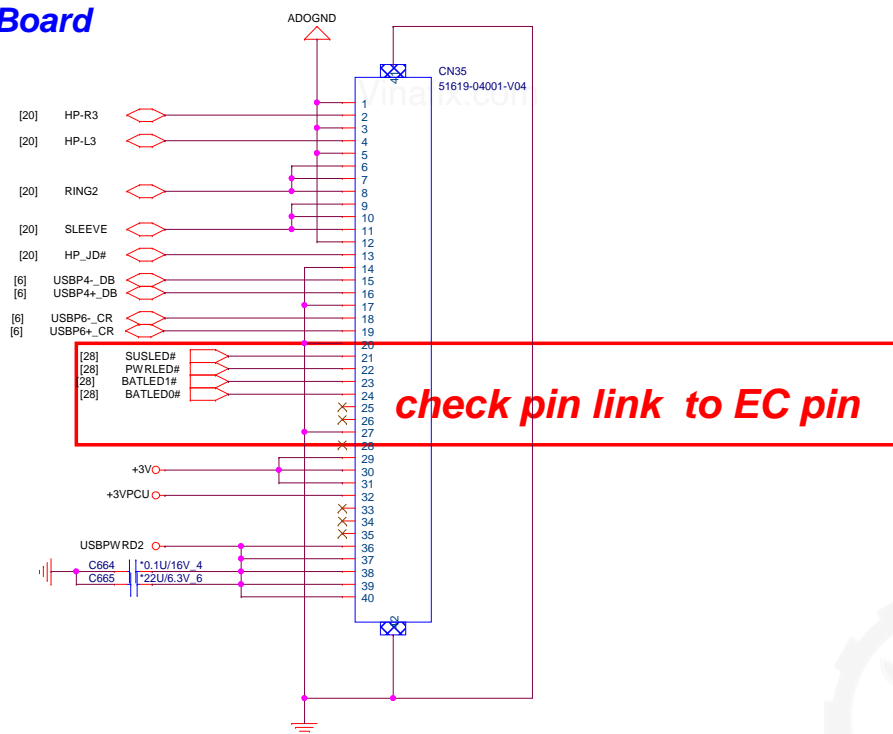
Reset SW (FSW)



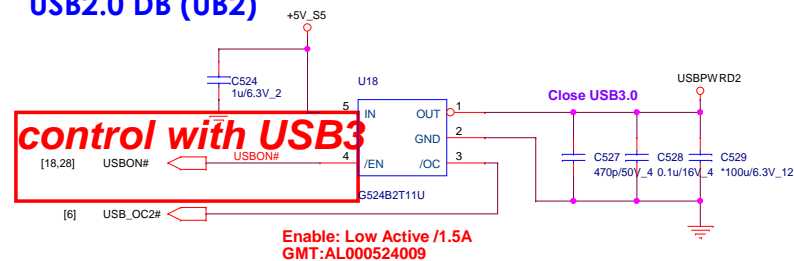
HW ID (A5 A3)



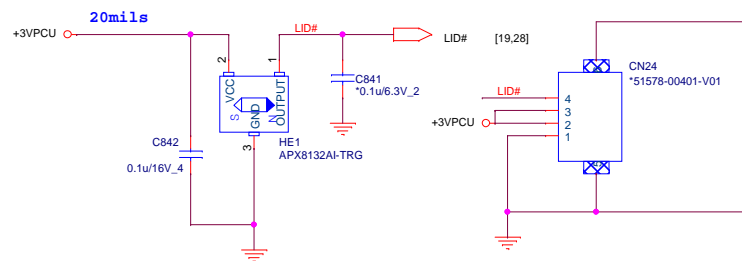
USB Board



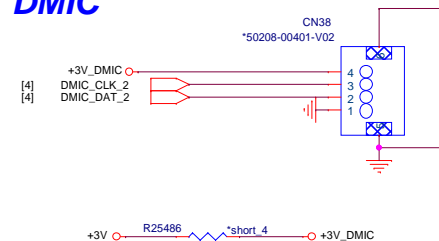
USB2.0 DB (UB2)



Hall Sensor



DMIC




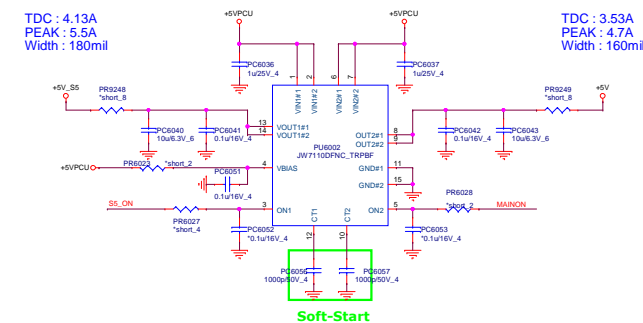
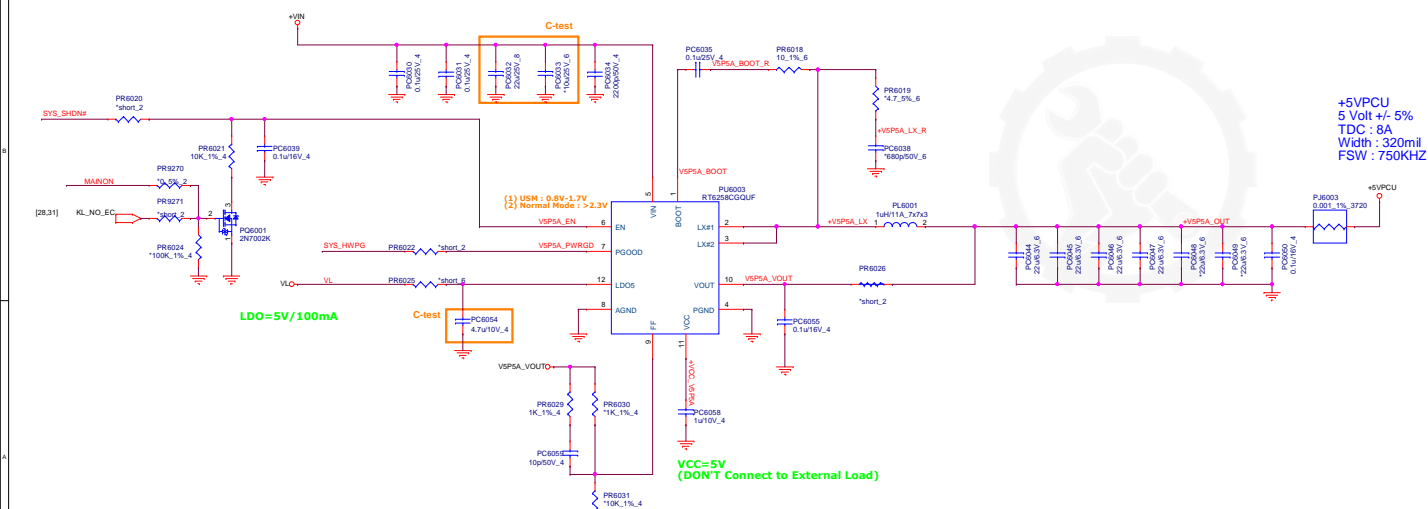
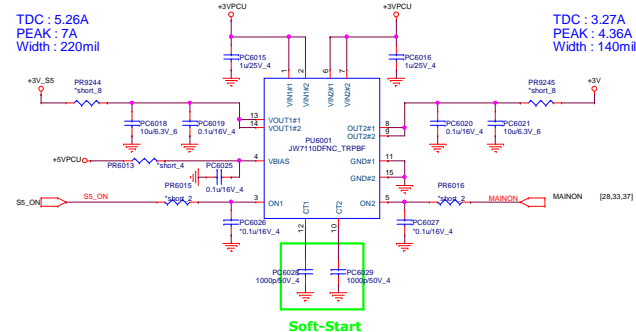
Quanta Computer Inc.

PROJECT : ZAU

Size	Document Number	Rev
	USB DB/Hall sensor/DMIC	1A

Date: Wednesday, April 10, 2019 Sheet 29 of 43

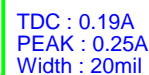
 Quanta Computer Inc. PROJECT : ZAU		
Size	Document Number Charger (BQ24780S)	Rev
Date:	Wednesday April 10 2019	Sheet 30 of 43



+1V_S5
1.0 Volt +/- 5%
TDC : 8.09A
Width : 340mil



Delete



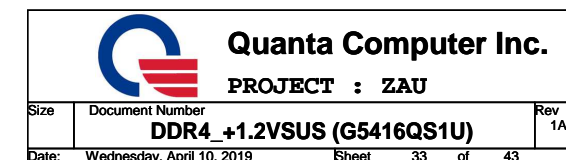
PROJECT : ZAU

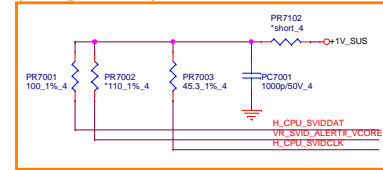
Rev	1A
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Date: Wednesday, April 10, 2019 Sheet 32 of 43

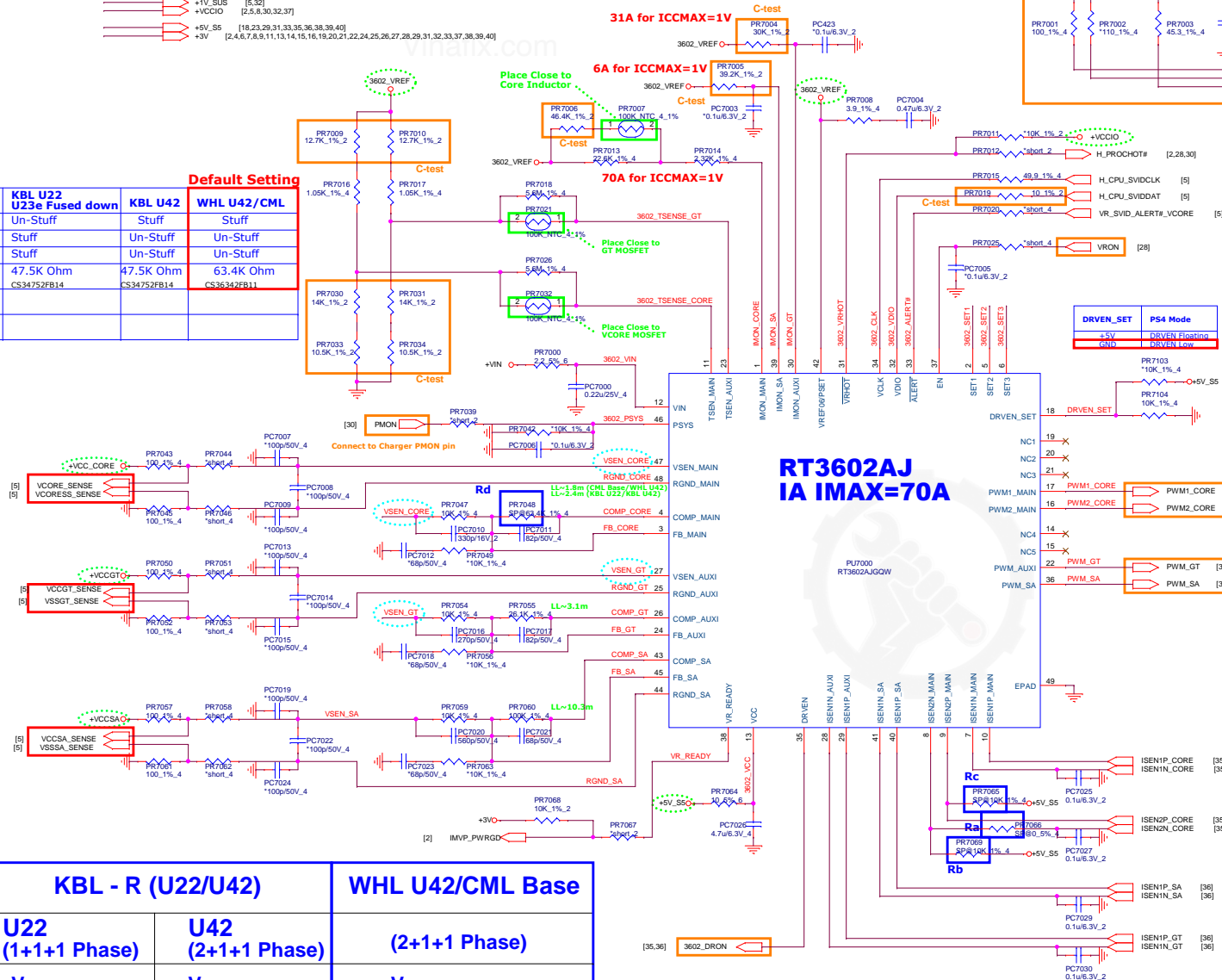


	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

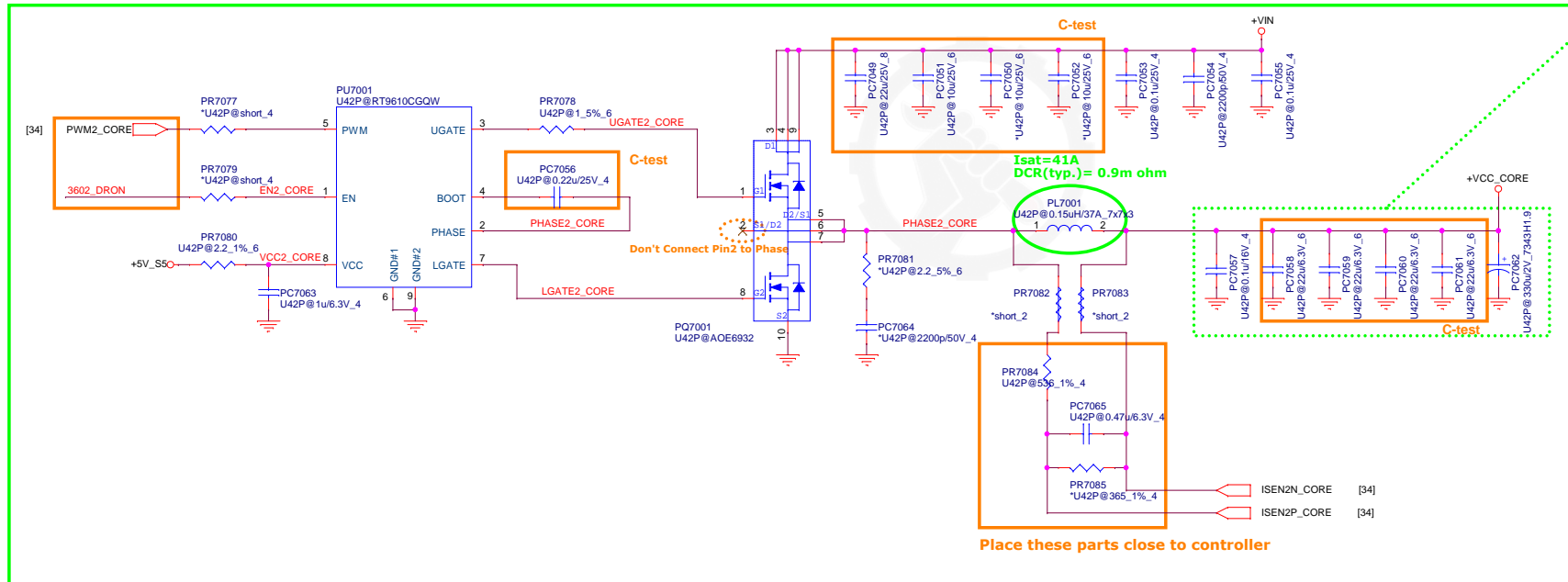
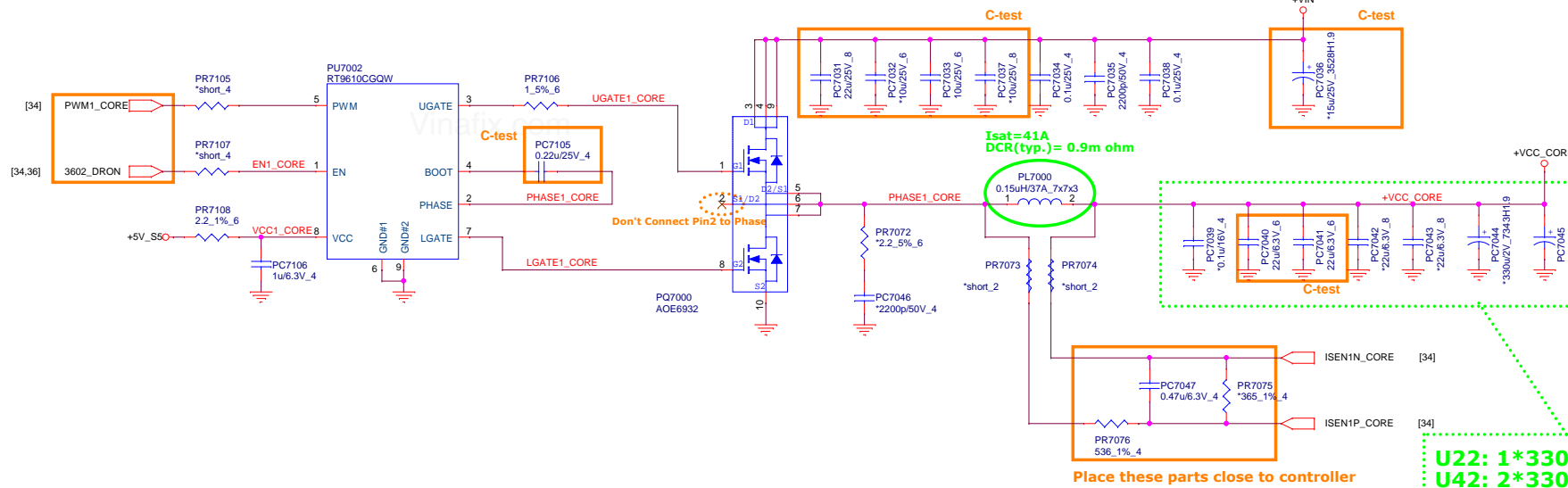




	KBL U22 U23e Fused down	KBL U42	WHL U42/CML
Ra	Un-Stuff	Stuff	Stuff
Rb	Stuff	Un-Stuff	Un-Stuff
Rc	Stuff	Un-Stuff	Un-Stuff
Rd	47.5K Ohm CS34752FB14	47.5K Ohm CS34752FB14	63.4K Ohm CS36342FB11
Rc			



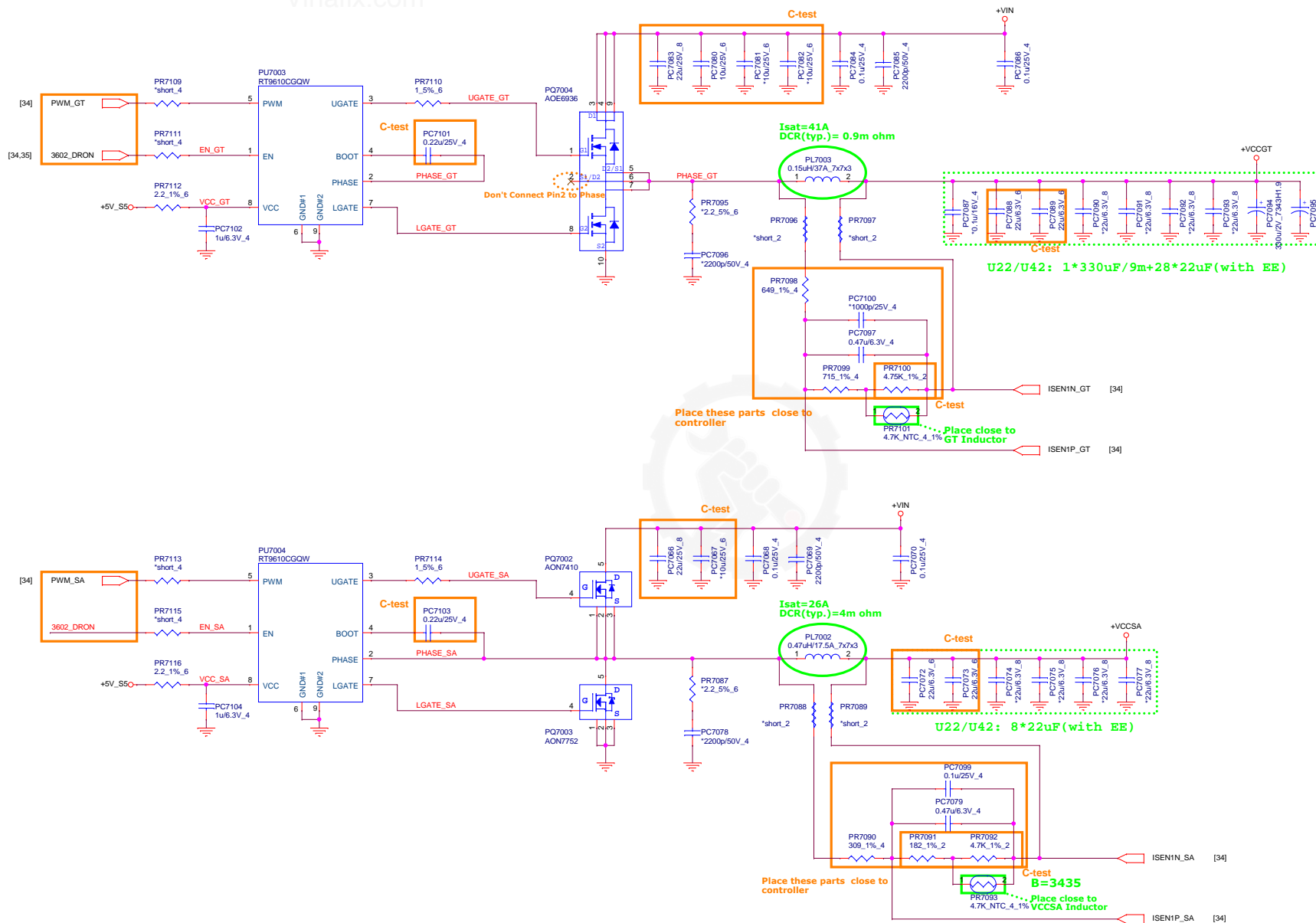
KBL - R (U22/U42)		WHL U42/CML Base
U22 (1+1+1 Phase)	U42 (2+1+1 Phase)	(2+1+1 Phase)
Vcore lcc Max : 32A lcc TDC : 21A OCP : 50A	Vcore lcc Max : 64A lcc TDC : 42A OCP : 100A	Vcore lcc Max : 70A lcc TDC : 48A OCP : 100A
VCCGT lcc Max : 31A lcc TDC : 18A OCP : 50A	VCCGT lcc Max : 31A lcc TDC : 12A OCP : 50A	VCCGT lcc Max : 31A lcc TDC : 18A OCP : 50A
VCCSA lcc Max : 6A OCP : 10A	VCCSA lcc Max : 6A OCP : 10A	VCCSA lcc Max : 6A OCP : 10A



		CPU	Power	Phase	Note
i3 i3-8130U BGA 2.2G Kaby Lake	AJSR3W0UT02	U42 (cost down)	15W	1+1+1	No staff U42P@
i5 i5-8250U BGA Kaby Lake KBL-R	AJSR3LAVT04	U42	15W	2+1+1	Staff U42P@

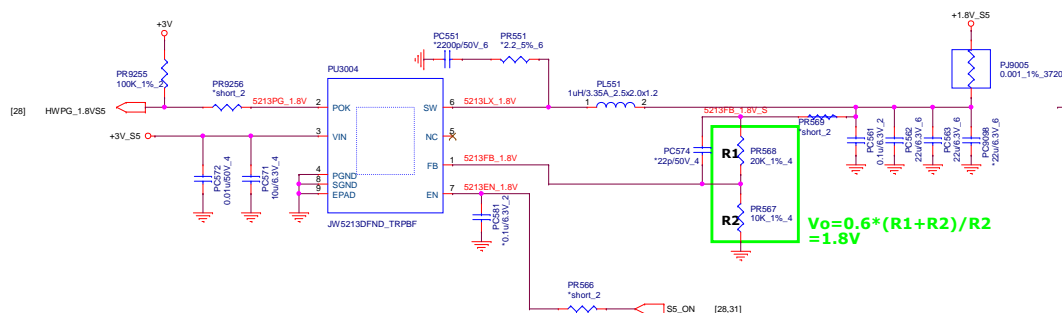
+VIN [19,30,31,32,33,34,35,37,38,39,40]
 +VCCGT [5,34]
 +VCCSA [5,34]
 +5V_S5 [18,23,29,31,33,34,35,38,39,40]

Vinafix.com



Vinafix.com

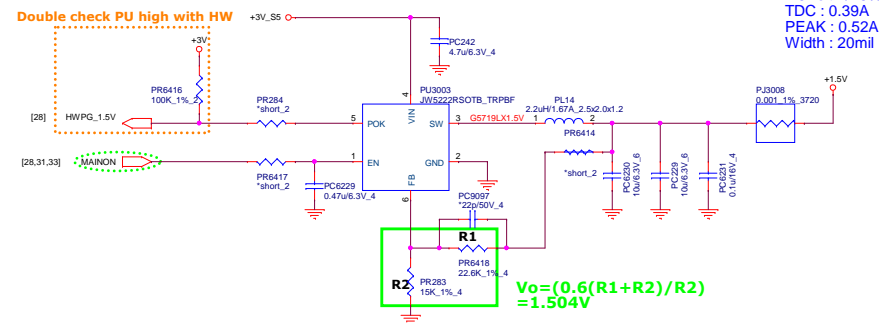
+1.8V_S5
1.8Volt +/- 5%
TDC : 2.48A
PEAK : 3.3A
Width : 100mil



$$V_o = 0.6 * (R1 + R2) / R2 = 1.8V$$

+1.8V_S5
TDC : 0.3A
PEAK : 0.4A
Width : 20mil

Double check PU high with HW

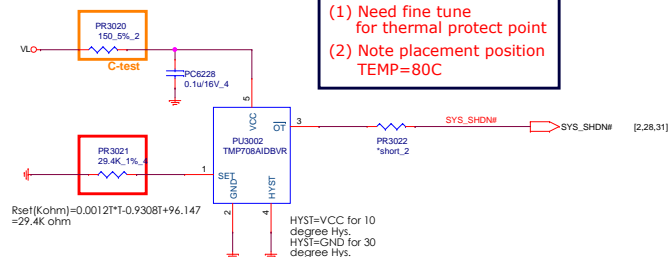


$$V_o = (0.6(R1 + R2) / R2) = 1.504V$$

+1.5V
1.5Volt +/- 5%
TDC : 0.39A
PEAK : 0.52A
Width : 20mil

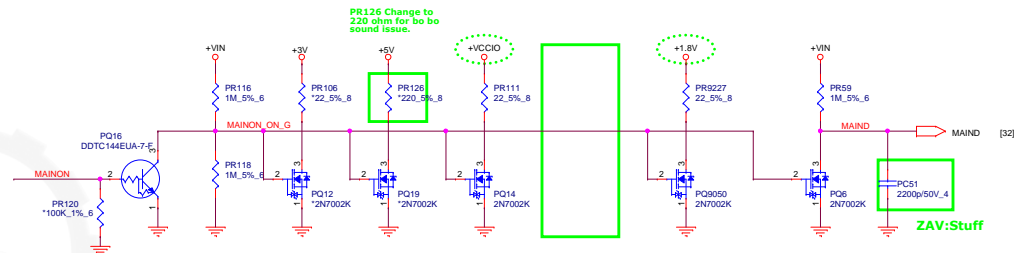
Thermal protection

- (1) Need fine tune for thermal protect point
- (2) Note placement position TEMP=80C



$$R_{set}(Kohm) = 0.00121 * T - 0.93087 + 96.147 = 29.4K \text{ ohm}$$

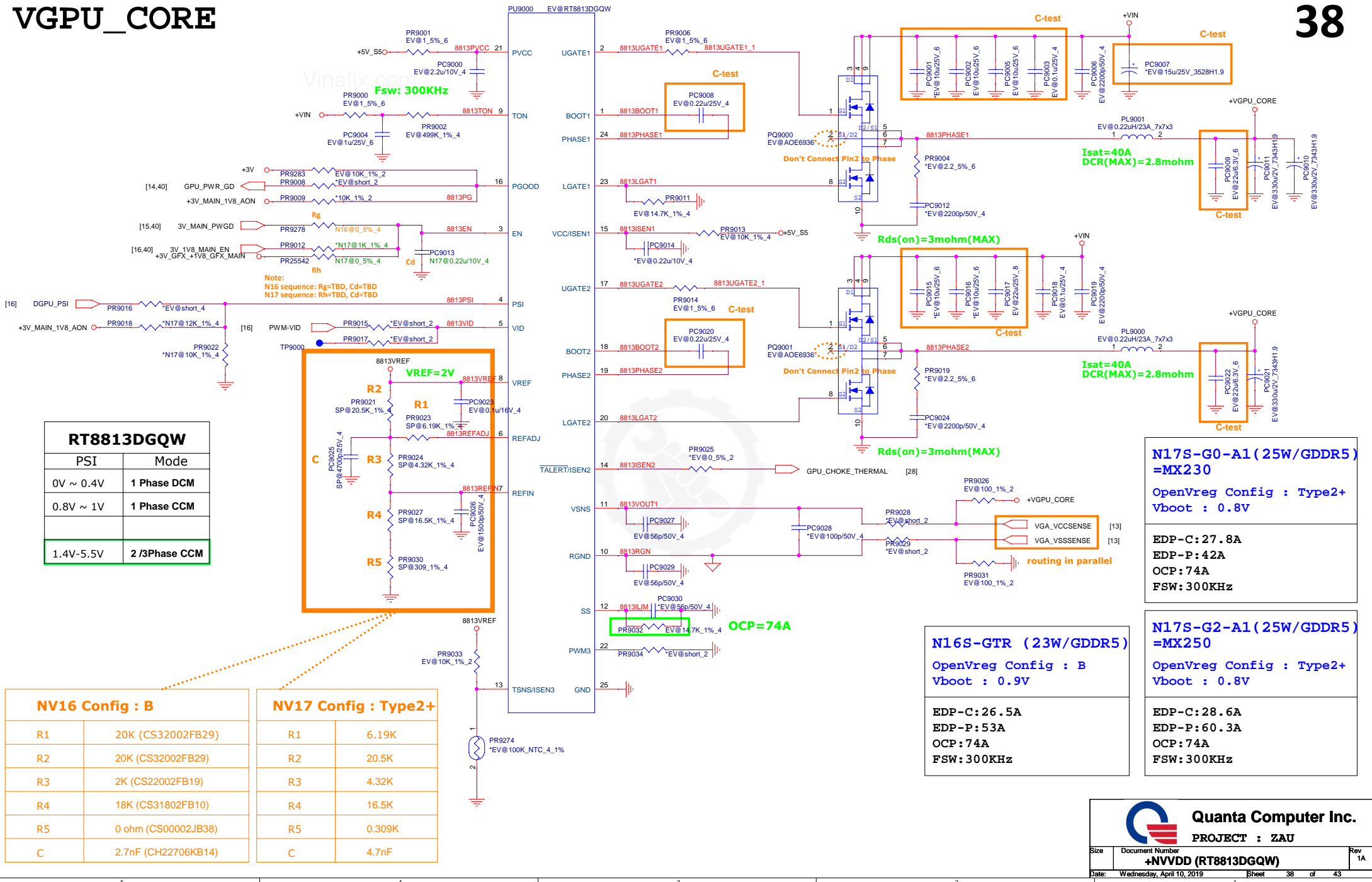
HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

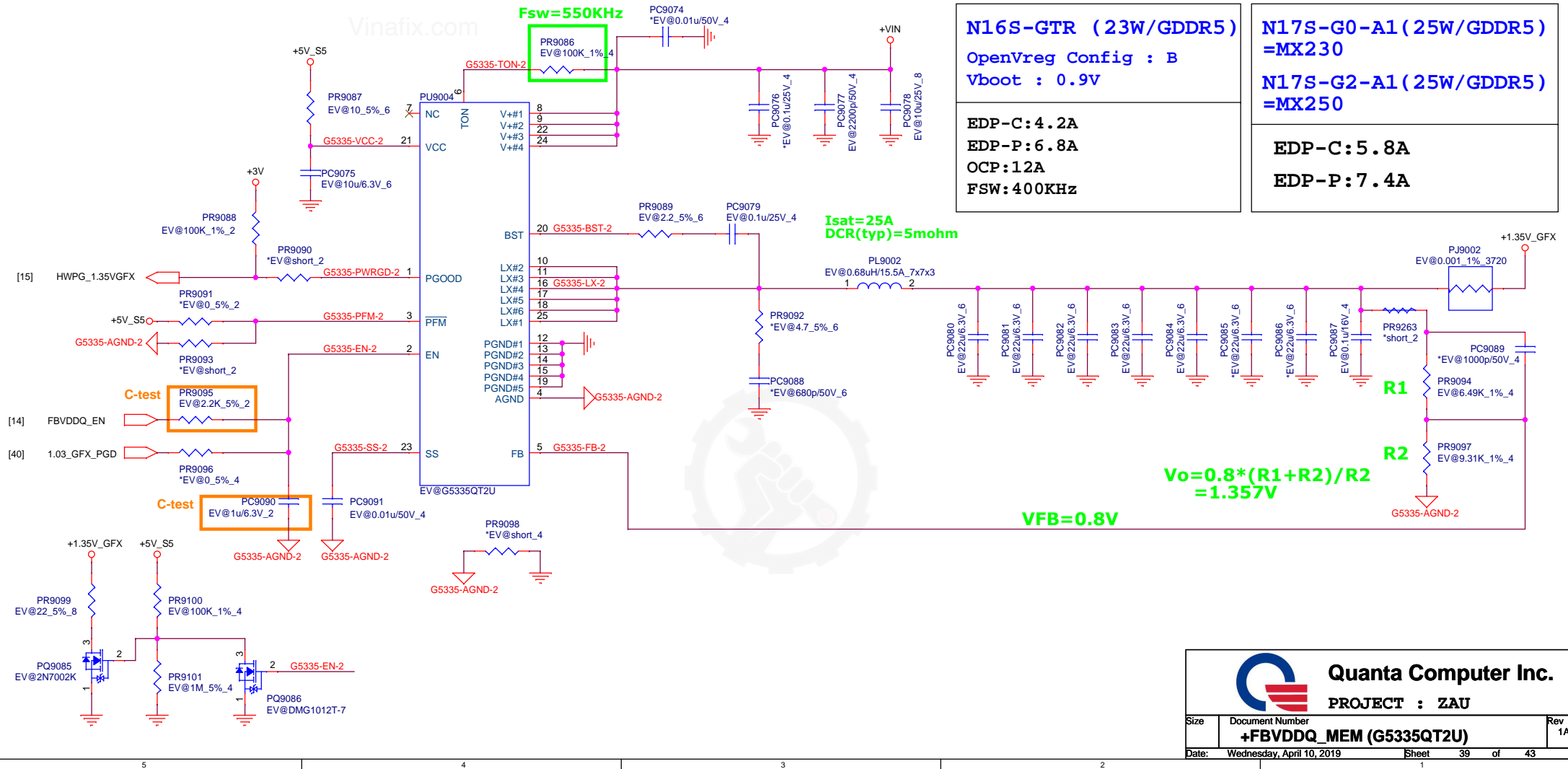


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PROJECT : ZAU

Size	Document Number	Rev
	+1.8V_S5/+1.5V/Thermal Protect	1A
Date:	Wednesday, April 10, 2019	Sheet 37 of 43

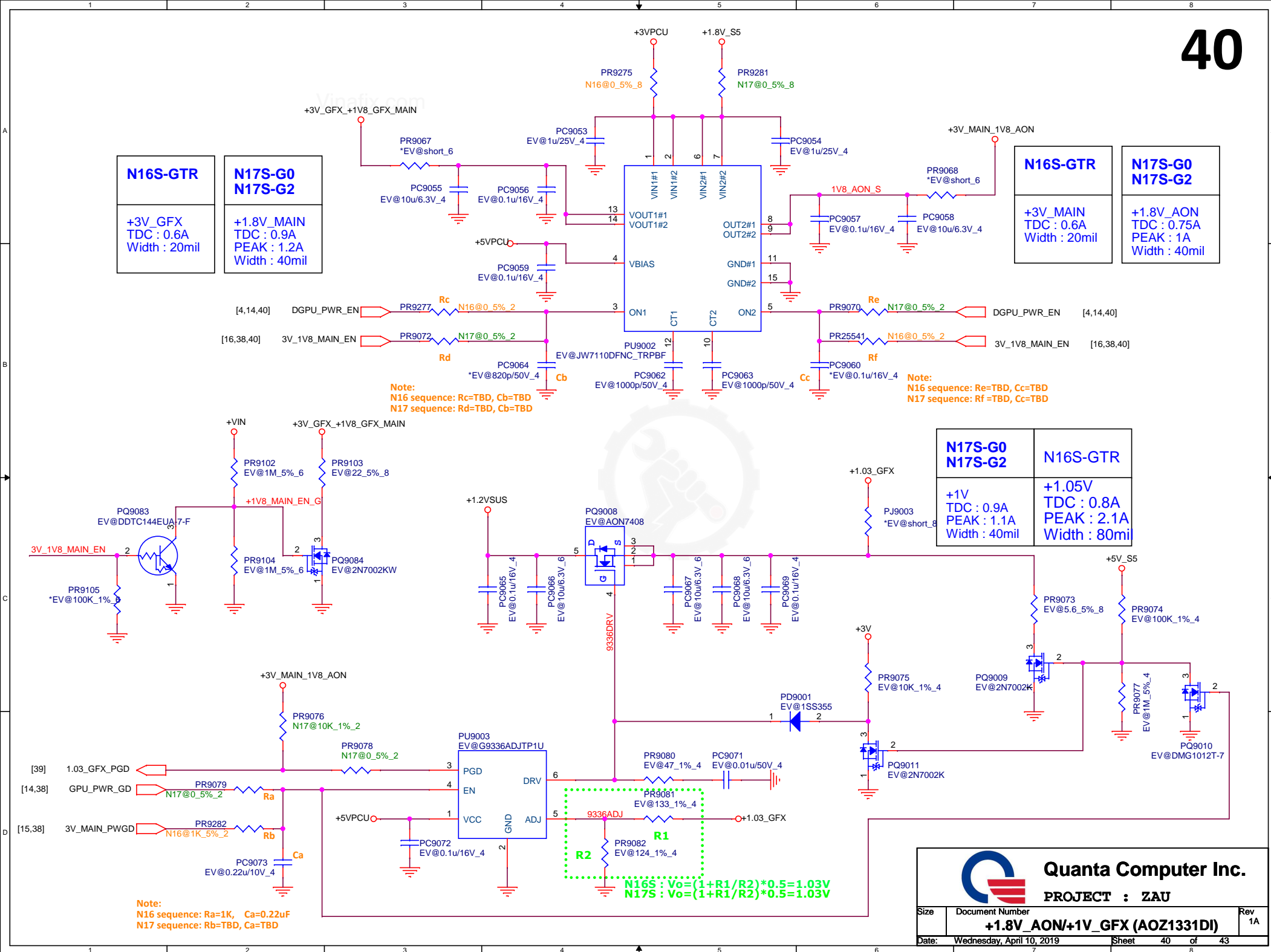




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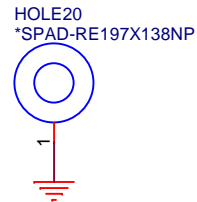
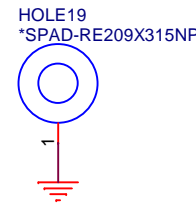
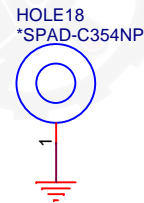
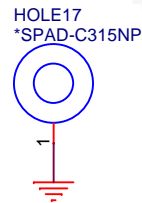
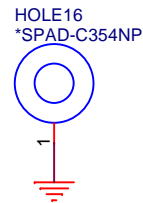
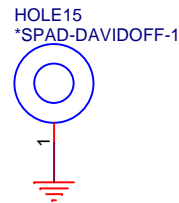
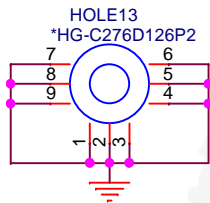
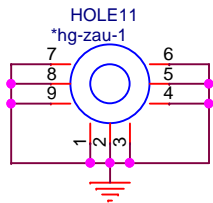
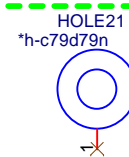
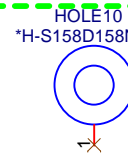
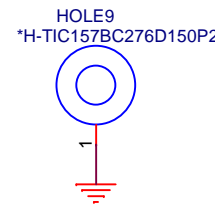
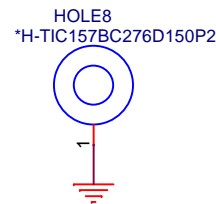
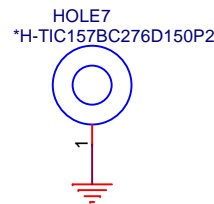
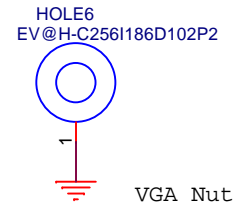
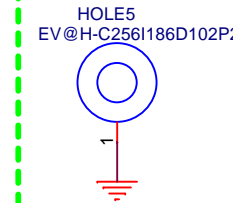
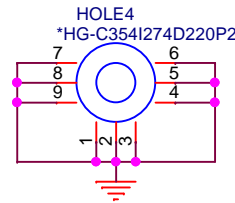
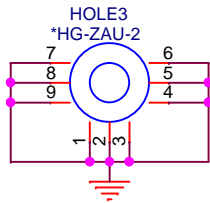
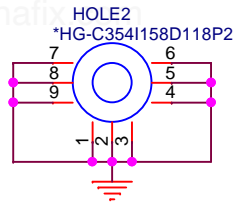
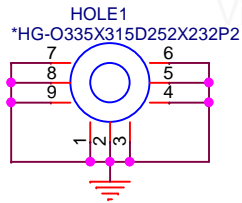
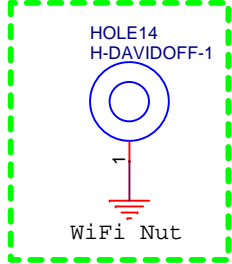
PROJECT : ZAU

Size	Document Number	Rev
	+FBVDDQ_MEM (G5335QT2U)	1A
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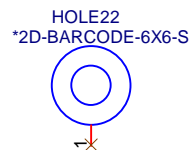
Hole


41



PAD

2D Bar Code(Only BOT Side)



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Model		Date	CHANGE LIST	
ZAV MP-stage	06/07	1. Delete L13,L14,L15 circuit. Add U38. (page 16)	42	
	06/08	1. Remove TXC_HDMI EMI Solution. (page 16)		
	06/09	1. Remove R873, R874. (page 16)		
		2. Remove L16, Change R775 from 0ohm to short. (page 16)		



